Dynamic voltage support by TL-PV systems to mitigate short-term voltage instability in residential DN

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Abstract—Recently, transformerless (TL) inverters are being extensively used in small-scale photovoltaic (PV) systems due to their compact-size, lighter-weight, lower-cost and higher-efficiency compared to their counterpart with transformer. However, the growing penetration of these small-scale based PV systems and low-inertia induction motor (IM) loads in low-voltage distribution networks (DNs) make the grid more vulnerable to short-term voltage stability (STVS). Hence, this paper thoroughly examines the STVS of DN with high-penetration of TL-PV units, and provides countermeasures by TL-PV systems to mitigate any short-term voltage instability (STVI). The detailed dynamic model of the TL inverter is developed first. Next, three control strategies: (1) constant peak current (CPC), (2) constant active current (CAC), and (3) constant active power (CAP) with low voltage ride through (LVRT) and dynamic voltage support (DVS) capabilities are proposed to improve STVS. The impacts of different level of PV penetrations and LVRT capability of TL-PV inverters on the STVS are explored. Moreover, countermeasures such as LVRT with CAC and CAP controls and DVS by the TL-PV systems are designed and implemented. Several case studies are carried out on an IEEE 4 bus system first, and later extended to IEEE 13 node test feeder. The results show that DVS can further improve STVS in residential DNs. In addition, CAP and CAC control strategies can speed-up the post-disturbance voltage recovery compared with the conventional CPC control.

Index Terms— Dynamic voltage support, fault induced delayed voltage recovery, low voltage ride-through, short-term voltage stability, transformerless inverter.

I. INTRODUCTION

In the recent decade, world has experienced a massive growth in PV installations and efforts are being made to achieve further growth. The total amount of PV installations including rooftops and other types has surpassed the landmark of 300 GW at the end of 2016 [1]. This trend of accelerating PV penetrations into the power systems more specifically in DNs may lead to an unwanted consequence of increasing the probability of DN's instability unless it is controlled properly.

With the increasing proportion of IM load, electronically controlled load, and introduction of power electronics based distributed generators (DGs) such as PV systems, STVS has become a subject of significant interest. Generally, short-term voltage instability (STVI) involves fast and complex load dynamics, and occurs in the time frame of few seconds [2]. There are mainly two types of STVI problems: (i) fault induced delayed voltage recovery (FIDVR) and (ii) voltage instability [3, 4]. FIDVR is a phenomenon whereby post-contingency voltage remains at considerably reduced level for several seconds [5]. On the other hand, voltage instability occurs while the post-contingency voltage reduces further and cannot be

recovered. Voltage instability is the prior stage of voltage collapse that may lead to a blackout in an area [4].

It has been concluded in several researches that the root cause of STVI is the stalling of IM loads following a disturbance [6-8]. In general, single-phase IM loads having low inertia such as air-conditioner compressor represent approximately 60-70 percent of peak load during hot weather in a residential grid [9]. An IM load draws 3-5 times of its rated current during stall that could prevent voltage recovery and may lead to rapid voltage collapse [3, 10, 11]. Another cause of STVI of highly PV-penetrated DN could be the dynamic behaviors of the PV systems itself [12, 13].

In order to mitigate STVI, two types of effort have been mainly devoted. One of them focuses on the demand side solutions which is mainly related to the employment of protection devices to rapidly disconnect the motor loads during slow voltage recovery [14, 15]. Implementation of this method can improve the STVS, but the system will experience some load shedding which is the main disadvantage of this method. Another type emphasizes on the supply side solutions that predominantly include reactive power support through DGs and flexible AC transmission system (FACTS) devices [3, 16-18]. By implementing this method, the STVS of a power system can be improved without load shedding. However, installing of extra compensating FACTS devices, namely static VAR compensator (SVC) or static synchronous compensator (STATCOM) will introduce additional cost. On the other hand, DG units are already existent in the network. Therefore, reactive power support by DG units for example PV systems has become the most attractive solutions for STVI problems.

Numerous studies have been conducted to examine the impact of IM loads on the STVS [6, 7, 14], as well as to explore the application of FACTS devices to improve the STVS [3, 16, 17]. In contrast, the impacts of dynamic behaviors of PV systems on the STVS have been discussed in very few researches [10, 12]. Voltage stability for residential customers due to high PV penetration has been investigated in [9]. It has been shown that loss of PV power due to cloud coverage has severe impact on the voltage stability of low-voltage DNs. Battery storage and PV reactive power support have been focused as potential solutions in [9]. In [10], the impact of sudden loss of PV power on the STVS is investigated for different scenarios of bus voltages. It has been concluded that STVI can occur in a slightly lower-voltage profile system [10]. However, the impacts of LVRT and DVS have not been taken into account in both of the research presented in [9, 10]. The effects of LVRT capability by PV-inverters have been examined in [12]. A conclusion has been drawn in [12] that STVS could be severely affected if the PV inverter trips-off or LVRT speed is lower following a large disturbance. However, the low-voltage DN and DVS with both active and reactive power injection have not been reflected in this paper.

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Fig 1. Advanced TL topologies: (a) HERIC topology [19] (b) H5 topology [20] (C) H6-type topology [21].

In the literature, most of the investigations on STVS have been carried-out in transmission or sub-transmission level. However, the DNs generally integrate small-scale PV systems (mainly single-phase rooftop PV), and the high efficiency and reliability are the main concerns of this type of PV systems. Recently, single-phase TL inverters are getting popular for small-scale PV application due to its higher-efficiency, lower-cost, lighter-weight and compact-size [19-24]. As the DNs are experiencing a large TL-PV penetration, it is important to ascertain whether the whole network is steady in regard to STVS or some adjustment is required. Therefore, a careful consideration on the dynamic performance of the TL-PV systems is required to ensure the consistent operation of DNs. Moreover, reliable and feasible countermeasures by TL-PV systems may become necessary to reduce the impact on the STVS in highly TL-PV penetrated DNs.

The main objective of this paper is to rigorously explore the STVS of DN based on different control strategies of TL inverter with LVRT and DVS capabilities. Firstly, the complete dynamic model of the TL-inverter is developed. Next, three control strategies: (1) CPC (2) CAC and (3) CAP are designed with LVRT and DVS capabilities. After that, the impact of different levels of TL-PV penetration on the STVS with conventional CPC control followed by the CAC and CAP control strategies with LVRT capability is investigated. It is observed that voltage instability in short-term is likely to happen for high PV penetrations. However, LVRT capability with conventional CPC control can prevent STVI, while CAP and CAC control schemes can further improve the STVS. Finally, in order to mitigate FIDVR, DVS by TL-PV inverters with different control schemes are provided as countermeasures. Case studies clearly show that DVS can speed-up the post-contingency voltage recovery process to avoid a possible STVI and voltage collapse. Furthermore, DVS with CAP control have better performance to improve STVS followed by the CAC and CPC control strategies, respectively.

The rest of the paper is organized as follows: the TL-PV systems have been modelled in details including the LVRT and DVS controls followed by the methodology to investigate STVS in Section II. Section III describes the results for the case studies that are carried out on the modified IEEE 4 bus system. Later, case studies are extended to IEEE 13 node test system to view the impact in unbalanced DN and for further validation of the results acquired in IEEE 4 bus system, and the results are given in Section IV. Finally, Section V accumulates the conclusions and contributions of this research.

II. MODELLING AND METHODOLOGY

A. Modelling of the transformerless PV inverter:

As a result of eliminating the transformer, an electrical connection has been established between the PV module and the grid in TL-PV grid connected inverter. Consequently, issues like leakage current and direct current (dc) injection can

be raised. In order to minimize leakage current and dc injection, several TL topologies as well as control strategies have been proposed [20-27]. Majority of these topologies has been derived from conventional full-bridge (FB) topology as shown in Fig. 1. The highest efficient topology has been proposed in [19] entitled “highly efficient and reliable inverter concept” (HERIC). This topology has been derived by adding two additional switches in the alternating current (ac) side of FB inverter as presented in Fig. 1(a). Fig. 1(b) depicts another promising topology called H5 inverter, where one extra switch has been added in the dc-side of FB inverter [20]. In order to reduce the current stress on the additional switch of H5 topology, H6-type topology which is shown in Fig. 1(c), has been proposed in [21]. It is worth mentioning that H6-type topology has been proposed with reactive power control capability, whilst H5 and HERIC topologies are required a slight modifications to deal with reactive power. In this research, TL topology presented in Fig. 1(c) is selected for the analysis due to its reactive power capability.

Overall control structure of the TL inverter is shown in Fig. 2. A new block consisting of dc-component extraction and an integral block of the virtual capacitor is added in the conventional direct-quadrature (dq) frame current control scheme [28]. In order to precisely control the output current as well as to reduce the dc injection, resonant controller is adopted with the proportional integral (PI) controllers. The dc-component is precisely extracted according to the average value method [28].

Fig 2. Overall control structure of TL-PV systems.

B. Low-voltage ride-through control:

Previously, the grid-tied converters had to be disconnected from the grid following a contingency to protect themselves from over-current. However, according to the several recently updated grid codes [23, 29-31], grid-tied converters are required to stay connected to the grid during the fault and preferably to recover the output after clearing the fault as soon as possible, which is defined as LVRT. It can be noted that in order to avoid any unintentional trip-off due to over current protection, output active power of the grid-tied inverter should be zero during the fault only, while the reactive power is always zero. In this research, LVRT control of the TL inverter is achieved by setting the reference value of the power controller as follows:

$$\begin{cases} \text{continue operation if } V_{gp} > 0.50 \text{ pu} \\ \text{to be remain connected with } P_{ref} = Q_{ref} = 0 \text{ if } V_{gp} \leq 0.50 \text{ pu} \\ \text{to be disconnected if } V_{gp} < 0.20 \text{ pu and } t \geq 0.2 \text{ s} \end{cases}$$

where V_{gp} is the instantaneous grid voltage in per unit (pu).

C. Dynamic voltage support control:

DVS by the grid-tied converters is defined as the ability of the converters to inject reactive power during fault instead of zero output as well as immediately after clearing the fault to support the grid voltage. The next generation grid-tied PV systems covering wide range of applications will be required to offer DVS [32]. In this research, DVS capability is perceived based on the active and reactive current injection strategies during voltage sag which is described in the following section in details.

D. Reactive current injection strategy:

It can be noted that the grid-tied inverter should inject sufficient reactive current in regard to the grid voltage condition during voltage sag. According to the E.ON grid code [32], the inverter should inject 100% reactive current when the grid voltage goes below 0.5 pu [32]. Reactive current I_q injection by the grid-tied inverter can be defined as:

$$I_q = \mu(1 - V_{gp})I_g \quad (1)$$

where I_g is the amplitude of grid current and μ is the reactive current scaling factor which is defined by (2).

$$\mu = \frac{(I_q - I_{q0})/I_g}{(1 - V_{gp})} \quad (2)$$

where I_{q0} is the initial reactive current before the fault. It is assumed that the TL-PV systems operate at unity power factor during normal operation ($0.95 < V_{gp} < 1.05$), thus the value of I_{q0} is set to be zero. According to the E.ON grid code, μ should not be less than 2 [32]. As seen in Fig. 3, 100% reactive current will be injected when the grid voltage reaches to 0.5 pu for $\mu = 2$.

Fig 3. Reactive current injection for $\mu = 2$.

E. Active current injection strategy:

According to the single-phase PQ theory, active power delivered to the grid can be written as follows:

$$P = \frac{1}{2} V_g I_g \quad (3)$$

where V_g is the amplitude of the grid voltage. As under normal operation ($0.95 < V_{gp} < 1.05$), the TL-PV inverters operate at unity power factor, the grid current in dq-frame and the active power would be:

$$I_d = I_g \quad (4)$$

$$I_q = 0 \quad (5)$$

$$P = \frac{1}{2} V_g I_d \quad (6)$$

The TL inverters should inject active power as well as reactive power following a disturbance to support the grid voltage. Therefore, the control strategy during a disturbance will be different to meet both active and reactive power injection. In this research, three types of controls are implemented with LVRT and DVS which are described below in details [32].

(i) *Constant peak current (CPC) control*: The maximum injected grid current I_{gmax} is always kept constant and equal to the inverter rated current during grid voltage sag with this control. According to this control strategy, the maximum current is defined in (7).

$$I_{gmax} = nI_n = \text{const.} \quad (7)$$

where I_n is the rated current of the TL-inverter, and n is the peak current scaling factor which has been introduced for derating operations. When the instantaneous grid voltage falls within the range of $(1 - 1/\mu) \leq V_{gp} \leq 0.95$, the grid current in dq-frame can be defined in (8) and (9).

$$I_d = \sqrt{n^2 - \mu^2 (1 - V_{gp}^2)} I_n \quad (8)$$

$$I_q = \mu(1 - V_{gp}) I_n \quad (9)$$

On the other hand, the grid current in dq-frame can be expressed in (10) and (11) if a severe fault occurs and the instantaneous grid voltage become $V_{gp} < (1 - 1/\mu)$.

$$I_d = (\sqrt{n^2 - 1}) I_n \quad (10)$$

$$I_q = I_n \quad (11)$$

(ii) *Constant active current (CAC) control*: According to this control, the active current is always kept constant for all circumstances regardless of grid voltage condition. From (6), the active current can be derived in (12) with respect to this control.

$$I_d = \frac{2P}{V_g} = mI_n = \text{const.} \quad (12)$$

where m is defined as the active current scaling factor for design considerations in case of derating operations. When the instantaneous grid voltage is within the range $(1 - 1/\mu) \leq V_{gp} \leq 0.95$, the grid current in dq-frame under this control mode can be expressed by (13) and (14).

$$I_d = mI_n \quad (13)$$

$$I_q = \mu(1 - V_{gp}) I_n \quad (14)$$

On the contrary, if severe fault occurs and the instantaneous grid voltage goes further below $(1 - 1/\mu)$, the grid current in dq-frame would be as in (15) and (16):

$$I_d = mI_n \quad (15)$$

$$I_q = I_n \quad (16)$$

(iii) *Constant active power (CAP) control*: The average active power is always kept constant during the whole period of grid voltage sag when the PV systems operate under this control mode. According to this control:

$$P = kP_n = \frac{1}{2} V_g I_n = \text{Const.} \quad (17)$$

where k is the derating factor, P_n is the nominal power. When the instantaneous grid voltage is within the range $(1-1/\mu) \leq V_{gp} \leq 0.95$, the grid current in dq-frame can be written in (18) and (19).

$$I_d = \frac{k}{V_{gp}} I_n \quad (18)$$

$$I_q = \mu(1-V_{gp}) I_n \quad (19)$$

Nevertheless, if the faults are severe and the instantaneous grid voltage becomes $V_{gp} < (1-1/\mu)$, the grid current in dq-frame would be:

$$I_d = \frac{k}{V_{gp}} I_n \quad (20)$$

$$I_q = I_n \quad (21)$$

(iv) *Comparison among the control strategies:* In order to thoroughly understand the differences among three types of active current injection strategies, amplitude of injected grid current I_g , and active I_d and reactive I_q currents are calculated according to these controllers, and plotted in Fig. 4 when $\mu=2$, $k=1$, $m=1$ and $n=1$. It can be observed from Fig 4(a) that I_g is limited within 1.0 pu and 1.43 pu for the controllers CPC and CAC respectively, while it exceeds 2.23 pu at 0.5 pu grid voltage with CAP strategy. Therefore, the possibilities of inverter trip-off due to over-current protection are high in CAP control when grid voltage is very low. It needs to be mentioned that most of the inverters are designed with maximum allowable current that allows it to operate with higher than rated loading condition for a certain period [32]. Consequently, a careful attention is required while designing the CAP control. Furthermore, as can be observed from Fig. 4(b), active current goes to zero at 0.5 pu grid voltage with CPC control whilst it has been kept constant for CAC scheme. In order to maintain constant active power in CAP strategy, active current increases with the voltage drop. In contrast, reactive current injection is identical for all control strategies as seen in Fig. 4(b).

Fig 4. Comparison of the three control strategies: (a) injected grid current and (b) active and reactive currents.

F. Short-term voltage stability:

It is common practice to carry out STVS studies using time domain simulations (TDS). However, to quantitatively examine the severity of STVI, an index has been proposed in the literature [33]. Therefore, in this research, TDS are carried out first, and later the index which is proposed in [33] are applied for further evaluation as well as to compare the STVS performance. In this paper, TDS are performed considering the detailed dynamic model of the TL-PV systems and the IM loads.

(i) *STVS assessment with index:* The magnitude of unacceptable transient voltage dip and duration of time has been defined in some industrial criteria [34]. However, it can

only provide a binary answer like whether the system was stable or unstable. Therefore, transient voltage severity index (TVSI) which was proposed in [33] is used to quantify the short-term voltage performance. TVSI can be defined in (22).

$$TVSI = \frac{\sum_{i=1}^N \sum_{t=T_c}^T TVDI_{i,t}}{N*(T-T_c)} \quad (22)$$

where N is the total number of buses, T and T_c are the considered transient time-frame and fault clearing time respectively, and TVDI is the transient voltage deviation index which is defined by (23).

$$TVDI_{i,t} = \begin{cases} \frac{V_{i,t} - V_{i,0}}{V_{i,0}} & \text{if } \frac{V_{i,t} - V_{i,0}}{V_{i,0}} \geq \gamma \\ 0 & \text{otherwise} \end{cases} \quad \forall t \in [T_c, T] \quad (23)$$

where $V_{i,t}$ is the voltage magnitude of bus i at time t , and γ is the threshold voltage. It can be noted that higher TVSI value reflects lower STVS level [33].

Fig 5. Modified IEEE 4 bus system.

III. CASE STUDIES ON IEEE 4 BUS SYSTEM

In order to investigate the impact of dynamic behaviors of TL-PV systems on STVS, several case studies are carried out for different scenarios in both balanced and unbalanced distribution systems. A modified version of the IEEE 4 bus system as shown in Fig 5 is used for the case studies which represents a balanced low-voltage DN. The PV systems and the aggregated loads are connected at bus 4 through a transformer that introduces a new bus 5. As the PV systems and the loads are connected at bus 5, it is referred as point of common coupling (PCC). The per-unit impedance for the new transformer (Tr2) is assumed to be the same as transformer 1 (Tr1). The loads are modelled as aggregated composite loads consisting of constant current, constant impedance and constant power (ZIP-type), and IM-type. In general, the loads are the combination of 25% ZIP-type and 75% IM-type in case of residential areas, although it can vary depending on the areas, seasons and time of the day [9]. In this research, in order to observe the effect of loads, case studies are accomplished with constant power (CP) loads first followed by high percentages of IM loads (75%) to focus on the STVS [12]. The per-unit parameters of IM loads are given in Table VIII in appendix A [35]. In order to accommodate the IM loads, the original loads of the IEEE 4 bus system have to be modified. The modified loads are given in Table IX in appendix A. All the pu calculations are accomplished with 1000 kVA base.

A. Impact of PV penetration and LVRT capability:

In this section, the STVS is investigated for different level of PV penetrations while the PV systems trip-off after a severe contingency followed by the LVRT capability of TL inverters with CPC control. The case studies are carried out by creating a three-phase to ground (3LG) fault at bus 1 for the duration of 0.2s. The short circuit capacity (SCC) is designated to be 105 MVA. The PV penetration level is calculated by (24). Four types of cases are considered for this investigation as shown in

Table I. Cases 1 to 3 are based on the PV penetration level while Case 4 implies the LVRT capability of TL-PV systems. The voltage profile at PCC are maintained at 1.03 pu before the fault by adjusting reactive power through shunt capacitors connected at buses 2 and 4 as shown in Table I. The variation of shunt capacitors can be observed in Table I owing to different initial power flow conditions for different penetration levels.

$$PV \text{ Penetration Level} = \frac{\text{Injected PV Power}}{\text{Total Load}} * 100 \quad (24)$$

Table I: Penetration levels and shunt capacitors.

Cases	Penetration level (%)	LVRT	Q_c (pu)	
			Node 2	Node 4
1	0	×	0.60	0.78
2	25	×	0.40	0.60
3	50	×	0.20	0.42
4	50	✓	0.20	0.42

The active and reactive powers and the voltage profile with CP loads are shown in Fig. 6. It is clear from Fig. 6(a) that before the fault, PV penetration level is achieved as described in Table I. Nevertheless, as soon as the fault is cleared at 1.2s, the TL-PV systems recover the output power in Case 4, while keeps zero injection in other cases. It can be perceived from Fig. 6(b) that the system is capable of recovering the post-contingency voltage for all the cases. However, low voltage profile can be observed after clearing the fault in Cases 3 and 4 which is due to the loss of PV power.

Fig 6. (a) Active and reactive powers and (b) dynamic voltage profile at PCC with constant power load.

Fig 7. (a) Active and reactive powers and (b) dynamic voltage profile at PCC with high percentage of IM loads (75%).

Fig. 7 depicts the active and reactive powers delivered by the TL-PV systems and the voltage dynamics at PCC with 75% IM load and 25% ZIP load. Witnessed by Fig. 7(a), active and reactive powers meet the required PV penetration levels as well as the LVRT conditions which are given in Table I. As expected, the dynamic behavior of PV output power is similar to the previous scenario with CP loads excluding Case 4. The TL-PV systems were unable to recover the output power immediately after clearing the fault with high IM load in Case 4. This is happened due to momentary low voltage and

constant peak current strategy. It can be noticed from Fig. 7(b) that due to a 3LG fault at bus 1, the voltage at bus 5 dropped to approximately 0.27 pu. However, after clearing the fault, FIDVR can be observed for the cases of high PV penetration levels. Consequently, STVI is likely to happen for high PV penetrations without LVRT capability of the inverter in Case 3 that can lead to fast voltage collapse. In contrast, the system is capable to recover the post-contingency voltage in Case 4 when the TL-PV systems ensure LVRT capability as observed in Fig. 7(b).

There are two possible reasons of STVI while the PV penetration levels are high. One could be high P and Q drawn by the IM trying to get back to normal operation, results in high line current and further voltage drop. Another one is the loss of PV power that needs to be supplied from the substation. In case of zero penetration level, only the first reason is valid, thus fast voltage recovery to the normal operation has been ensured. Furthermore, in Case 4 with 50% penetration, fast voltage recovery to the normal operation has been ensured since PV power loss occurred during the fault only and recovered nearly after the fault is cleared.

The TVSI for different cases are calculated and tabulated in Table II according to (22). During calculation, the parameters are set as follows: $N=5$, $T=2s$, $T_c=1.2s$, $step \ time=2\mu s$, and $\gamma=20\%$. As seen in Table II, TVSI values are very low and close for all the cases with CP load, indicating no STVI issues for different PV penetrations. However, the TVSI values are increased for Cases 1 to 3, whilst lowest value is observed in Case 4 with high IM load. Therefore, it is clear that the STVS has been impaired with the increased penetration when the system are having high IM load. Nevertheless, in Case 4, the STVS is improved as the TL-PV systems are equipped with LVRT capability.

Table II: TVSI for different cases.

	Case 1	Case 2	Case 3	Case 4
CP loads	1936	1959	2021	2007
High IM loads	6992	27217	58683	3351

The conclusion can be drawn from this section is that the post-disturbance voltage could be recovered to normal value with CP loads in the studied systems. However, STVI is likely to happen with high PV penetrations if the loads are the combination of IM-type (75%) and ZIP-type (25%). It can be noted that IM loads in a residential grid during a sunny hot day in summer could be as high as 75 percentages of total loads [9, 12]. Therefore, in the following section, countermeasures are provided to avoid any short-term voltage instability considering a sunny hot day.

B. Countermeasures by TL-PV inverters:

It has already been shown that the STVI can be avoided for high PV penetrations when the TL-PV inverters are equipped with LVRT capability. However, the scenario could be different if the voltage profile is slightly lower and the system is relatively weak. Therefore, case studies are conducted with 1.0 pu pre-fault voltage profile in this section. The short-circuit capacity of the system is designed to be 100.0 MVA. It is observed that STVI can occur with high PV-penetration even though LVRT capability with conventional CPC control is provided. Therefore, countermeasures by TL-PV inverters are provided as solutions of STVI problems. At first, LVRT with

CAC and CAP controls is applied. Next, DVS with different control strategies are provided for further improvement of the STVS. Two types of faults are considered to verify the competency of the countermeasures which are listed below:
 Fault 1: 3LG fault occurred at bus 1 for the duration of 0.2s.
 Fault 2: 3LG fault ensued far from bus 1 in the upstream of the network and cleared after 0.3s.

(i) *LVRT capability with CAC and CAP controls:* In order to observe the effectiveness of this countermeasure, three types of scenarios are simulated as presented in Table III. Three scenarios are based on the CPC, CAC and CAP control strategies with LVRT capability.

Table III: Investigation scenarios.

Scenarios	LVRT	Control mode	PV Penetration
1	√	CPC	50 %
2	√	CAC	
3	√	CAP

Fig 8. (a) PV output power and (b) injected grid current for fault 1.

Fig 9. Dynamic voltage profile at PCC for fault 1.

The active and reactive powers, and the injected grid current delivered by the TL-PV inverters are presented in Fig. 8. It can be seen that before the fault, active power injection was same for all scenarios while reactive power injection is zero. However, once the fault is detected, active power injection becomes zero to satisfy the LVRT condition. After clearing the fault, the active power of the PV systems is recovered according to the respective controllers that can be notable from Fig. 8(a). As the PV systems are not equipped with DVS capability, reactive power injection is kept zero during the whole period. The voltage profile at PCC following fault 1 is shown in Fig. 9. Due to a 3LG fault, the PCC voltage drops to approximately 0.25 pu as witnessed by Fig. 9. However, the voltage is recovered for all scenarios after clearing the fault. It is clear that the fastest voltage recovery is ensured with CAP control, whilst identical recovery is observed for the CAC and CPC controls. This is due to the constant active power injection by the TL-PV systems into the grid instantly after clearing the fault with CAP control. On the other hand, equal amount of active power which is less compared to CAP control is injected

by the CAC and CPC controls. Furthermore, it can be noticed from Fig. 8(b) that injected grid current is limited within rated with CPC and CAC controls while it exceeds for CAP control. Therefore, a careful attention is required to design CAP control.

Fig 10. (a) PV output power and (b) grid current at PCC for fault 2.

Fig 11. Dynamic voltage profile at PCC for fault 2.

The PV output power and current, and the dynamic voltage profile at PCC for fault 2 are given in Figs. 10 and 11, respectively. Fault 2 is assumed more severe than fault 1 due to longer clearing time. It can be understood that unlike fault 1, voltage recovery is ensured only for Scenario 3 in case of fault 2, though FIDVR can still be observed. Consequently, PV output power is recovered with CAP control. Witnessed by Fig. 10(b), the output current behaviors are almost identical to fault 1 as expected. Because of longer clearing time, stalling IM loads reach to the critical speed for Scenarios 1 and 2 following fault 2, which resulted in short-term voltage instability as seen in Fig. 11.

Table IV represents the calculated values of TVSI for different scenarios. It can be seen that the values are very high and adjacent for Scenarios 2 and 3 with fault 2 as STVI occurs for both scenarios. However, for both faults, though the TVSI values are very close and high for Scenarios 1 and 2, it is comparatively reduced in Scenario 3, clearly indicates that the system has experienced better performance with CAP control.

Table IV: TVSI for different Scenarios.

	Scenario 1	Scenario 2	Scenario 3
Fault 1	17954	17889	7571
Fault 2	45216	45102	19820

Table V: Four types of cases based on the control method.

Case	LVRT	DVS	Control mode
1	√	×	CPC
2	√	√	CPC
3	√	√	CAC
4	√	√	CAP

(ii) *DVS by TL-PV inverters:* From the prior case studies, it is observed that LVRT even with CAP and CAC controls might not be effective to alleviate STVI issues while the

system encounters severe contingency. Therefore, in this section, DVS with different control strategies is provided as potential solutions to avoid any STVI as well as to mitigate FIDVR. In order to accomplish this task, four cases are investigated as listed in Table V. Case 1 is the base case characterized by CPC control with LVRT only, while Cases 2-4 are based on the CPC, CAC, and CAP controls with DVS capability.

Figs. 12 and 13 demonstrate the PV output power and current, and the voltage dynamics at PCC respectively. It can be seen that before the fault, active power injection was same for all cases. However, during the fault, active power delivered by TL-PV systems is zero for Cases 1 and 2. In contrast, the TL-PV systems inject active power approximately 33% and 100% of rated power in Cases 3 and 4. Consequently, injected grid current exceeds the rated current in Cases 3 and 4 as shown in Fig. 12(b). Witnessed by Fig 13, the system has experienced an uneven voltage drop owing to the 3LG fault at bus 1 as a result of unequal PV power injection. After clearing the fault, the variation of the output power with grid voltage can be observed subject to the corresponding controls in Fig. 12(a). It is clear that the voltage is recovered for all cases. However, the fastest voltage recovery to pre-fault value is observed for Case 4 since TL-PV systems deliver constant active power into the grid. On the other hand, voltage recovery is decelerated for the Cases 3 to 1 respectively due to reduced amount of active power injection into the grid.

Fig 12. (a) Active and reactive powers delivered by the TL-PV systems and (b) injected grid current for fault 1.

Fig 13. Dynamic voltage profile at PCC for fault 1.

The PV output power and current, and the dynamic grid voltage profile at PCC are shown in Figs. 14 and 15 when fault 2 has been ensued in the system. Witnessed by Fig. 15, the system has experienced STVI for Case 1, while voltage recovery has been confirmed for all other cases. However, worse FIDVR can be observed in Case 2 due to zero active power injection by the TL-PV systems during the fault and stalling of IM. On the other hand, it can be realized that DVS by TL-PV systems with CAP and CAC controls can improve FIDVR in Cases 3 and 4 since both active and reactive powers

have been injected into the grid during voltage sag. It can also be observed that the TL-PV systems were unable to recover the output for Case 1 due to STVI, while it faces delayed recovery for Cases 2 and 3 depending on the corresponding controls and grid voltage condition. Furthermore, as like fault 1 injected grid current exceeds rated value with CAC and CAP controls as seen in Fig. 14(b).

Fig 14. (a) Active and reactive powers delivered by the TL-PV systems and (b) injected grid current for fault 2.

Fig 15. Dynamic voltage profile at PCC for fault 2.

Table VI: TVSI for different cases.

	Case 1	Case 2	Case 3	Case 4
Fault 1	17954	4895	2501	1688
Fault 2	45216	5670	1591	1232

Table VI lists the TVSI values for the cases described in Table V for both of the faults. As observed from the comparison shown in Table IV and VI, DVS improves the STVS compared with LVRT capability for the identical contingency. As well, finest performance in enhancing the STVS has been attained with CAP control, followed respectively by the CAC and CPC controls, as reflected in simulation results.

Finally, from the case study, it can be perceived that DVS can be a potential solution to avoid short-term voltage instability instead of providing only LVRT capability. Furthermore, the voltage recovery process can be accelerated with CAP and CAC controls compared with CPC control.

IV. CASE STUDIES ON IEEE 13 NODE TEST FEEDER

Generally, the residential distribution system is inherently unbalanced due to its unbalanced load and line configuration. Therefore, in this section, the proposed countermeasures to mitigate STVI issues are verified in an unbalanced distribution system. The IEEE 13 node test feeder is chosen for the case studies as it represents an unbalanced residential DN. It is modified by including PV systems and IM loads. The details of the IEEE 13 node test feeder can be found in [36]. The SCC of the system has been designed to be 105 MVA. The load combinations are approximated to be 70% of IM-type and 30% of ZIP-type. The details of the modified loads are given in Table X in appendix A. The TL-PV systems are connected at

each phase of nodes 675, 671, 634, 611, 652 and 645 as shown in Fig. 16. The PV penetration levels at each node are tabulated in Table VII. As the nodes 611 and 675 are placed in the remote locations of the network and connected with large loads, these two nodes have been considered for STVS investigation. The voltage profiles at each node of the modified IEEE 13 node test feeder before the fault are illustrated in Fig. 17. It is clear that the voltages at all the nodes are between 0.95 pu to 1.05 pu. Therefore, the requirement for voltage profile stated in different international standard is satisfied.

Fig 16. Modified IEEE 13 node test feeder.

Table VII: PV penetration scenarios.

Bus no	675	671	634	611	652	645
Phases	A,B,C	A,B,C	A,B,C	C	A	B
PV power (pu)	0.2	0.1	0.1	0.2	0.2	0.2

Fig 17. Voltage profile of all phases at each node before the fault.

A. Impact of LVRT capability with CAC and CAP controls:

In order to analyse the impact of LVRT capability of TL-PV systems with CAC and CAP controls on STVS in IEEE 13 node tests feeder, case studies are conducted for the scenarios presented in Table III. Two types of fault are taken into consideration, which are described in Section III (B). It is assumed that Fault 1 is occurred at node 632, whilst fault 2 far away from node 650 in the upstream of the network. The voltage profile at nodes 675 and 611 are illustrated in Fig. 18 for fault 1. It can be seen that voltages of all phases have been recovered to its pre-fault value for all scenarios at node 675. However, the fastest recovery is observed for phase B, while phases A and C respectively have realized slow recovery. This is happened due to the network configuration. Most of the loads of phase B are connected to the upstream nodes. As well, the only remote load which is connected at node 675 is relatively small and compensated by 200 kVar capacitor bank. Therefore, higher voltage profile and fast recovery to pre-fault value has been recognized in phase B. In contrast, a number of remote loads are connected in phases A and C, which is the main cause of relatively lower voltage profile and slower recovery speed in these phases. However, worse voltage dynamics can be seen in phase C. This is owing to the total loading of phase C especially at the remote buses which is

much more than phase A. Furthermore, the voltage regaining process of phases A and B for different scenarios is almost identical. Thus the impacts of LVRT with CAC and CAP controls on STVS are very insignificant at strong nodes. In contrast, it can be seen from both Figs. 18(a) and 18(b) that the voltage retrieval process to the pre-fault value has been augmented for CAP control compared with CAC and CPC controls in phase C which is the weakest phase. This is due to the constant active power injection into the grid after clearing the fault with CAP control. Therefore, in the following investigations, the performance of phase C will be highlighted.

Fig 18. Dynamic voltage profile at node: (a) 675 and (b) 611 for fault 1.

Fig 19. Dynamic voltage profile at node: (a) 675C and (b) 611 for fault 2.

Fig. 19 depicts the voltage profile at nodes 675C (phase C of node 675) and 611 for fault 2. It is clear that STVI is likely to occur in this circumstance. Nevertheless, LVRT with CAP and CAC control strategies have not been capable to prevent STVI due to IM stall as witnessed by both Figs. 19(a) and 19(b).

B. Impact of DVS with CPC, CAC, and CAP controls:

In order to analyze the impact of DVS capability of TL-PV systems with CPC, CAC and CAP controls on the STVS, four cases are investigated which have been narrated in Table V. Figs. 20(a) and 20(b) illustrate the voltage dynamics at nodes 675C and 611 respectively for fault 1. As like the case study conducted in IEEE 4 bus system, voltages at both nodes have been restored to pre-fault value for all cases flowing fault 1. However, voltage regaining process has been accelerated for Case 4, whilst Cases 3, 2 and 1 respectively have experienced relatively slower recovery.

Fig 20. Dynamic voltage profile at node: (a) 675C and (b) 611 for fault 1.

The voltage profile at nodes 675C and 611 are presented in Fig. 21 while the system encounters fault 2. Both Figs. 21(a) and 21(b) indicate that STVI is likely to occur for Cases 1 and 2 due to IM stall and zero active power injection during fault by TL-PV systems. However, in Cases 3 and 4, the post-disturbance voltage is recovered to the pre-fault value, consequently STVS is improved.

Fig 21. Dynamic voltage profile at nodes: (a) 675C and (b) 611 for fault 2.

V. CONCLUSIONS

In this research, the impact of LVRT and DVS capability of TL-PV systems with three different control strategies on the STVS is investigated. Case studies are carried-out on two benchmark test systems i.e. IEEE 4 bus and IEEE 13 node test feeder for different scenarios. The results reveal that STVI is likely to occur for high PV penetration in residential DN having high IM loads if the PV systems trip-off due to disturbance. However, LVRT capability of TL inverters with conventional CPC control may prevent STVI in highly TL-PV penetrated DN, though FIDVR which is another concern of STVI problems can still be observed.

Therefore, in order to mitigate FIDVR, countermeasures by TL-inverters are proposed. One of the countermeasures is the LVRT with CAC and CAP controls. It is realized that post-disturbance voltage recovery process can be accelerated with CAP and CAC controls. However, in case of a worse situation for example fault 2 in this paper, the residential DNs might still experience poor FIDVR, and in some cases voltage instability. Therefore, another countermeasure which is DVS capability by TL-inverters with CPC, CAC and CAP control schemes is provided. It is clearly shown that the STVI can be mitigated if the TL inverters ensure DVS capability. Furthermore, fastest voltage recovery to pre-fault value has been ensured with CAP control, followed by the CAC and CPC controls, respectively. Therefore, it can be concluded that the STVS of DN can be severely impaired without appropriate design of the PV systems. Consequently, a careful consideration on the dynamic performance of PV systems and the design of appropriate controls are required, which is addressed in this paper. It is expected that this investigation will be helpful for DN design engineers' as well as the power system operators' to design a reliable highly PV-penetrated DN.

APPENDIX A

Table VIII: pu parameters of IM load [35]

R_s	X_s	R_r	X_r	X_m	H	p
0.1	0.1	0.09	0.06	2.5	.28	2

Table IX: Modified load of IEEE 4 bus system

Phase	kW		kVAr		kVA
	IM	ZIP	IM	ZIP	
A	765	320	481	35	1201
B	765	320	481	35	1201

C	765	320	481	35	1201
Total	2295	960	1443	105	3603

Table X: Modified loads of IEEE 13 bus system

Bus no	kW						kVAr					
	IM-type			ZIP-type			IM-type			ZIP-type		
	A	B	C	A	B	C	A	B	C	A	B	C
675	300	55	238	185	13	52	189	35	150	0	25	62
671	285	285	285	100	100	100	179	179	179	41	41	41
671 (DL)	0	40	85	17	26	32	0	25	53	10	13	15
634	119	102	102	41	18	18	75	64	64	35	26	26
611			119			51			75			5
652	102			26			64			22		
645		145			25			91			34	
646		0			230			0			132	
692			119			51			75			76
Total	806	627	948	369	412	304	507	394	596	109	271	225

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