Novel SiC Accumulation-Mode Power MOSFET

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Abstract—In this paper, a new structure of Silicon Carbide (SiC) accumulation-mode MOSFET (ACCUFET) for high-power applications has been proposed and analyzed. The novel ACCUFET utilizes fully depleted N-channel epilayer, grown on P-base epilayer, to achieve normally-off operation. A trench region is formed by etching and is implanted to create N-type path that connects the N-channel epilayer (accumulation channel) to underlying N-drift region. Detailed analysis of the important design parameters of the novel structure is performed using MEDICI two-dimensional (2-D) device simulator. The novel structure was also compared to alternative ACCUFET approaches, specifically planar and trench-gate ACCUFETs. The comparison shows that the novel structure provides the highest figure of merit (FOM) for power devices.

Index Terms—Device simulation, power MOSFET, Silicon Carbide (SiC).

I. INTRODUCTION

DUE TO excellent physical and electrical properties, such as high breakdown electric field, wide bandgap, high thermal conductivity, and high electron saturation velocity, Silicon Carbide (SiC) offers great potential for development of high-temperature, high-power, and high-voltage devices. On the other hand, the inherent MOSFET advantages make this class of devices an attractive direction for development of power devices with voltage ratings up to 3 kV [1]. Significant progress in SiC power MOSFETs have been demonstrated recently, with the fabrication of UMOS [2], DMOSFET [3], triple-implanted vertical MOSFET [4], RESURF MOSFET [5], and accumulation-mode MOSFETs (ACCUFETs) [6]–[9]. Recent ACCUFET developments [6]–[9] reveal important advantages of this type of MOSFET structure. ACCUFETs emerge as the preferred solution for power MOSFETs on SiC, because of their advantage in terms of higher channel-carrier mobility compared to the standard inversion N-type MOSFETs.

This paper proposes a new design of accumulation-mode power MOSFET and its optimization using MEDICI two-dimensional (2-D) device simulator. This paper also presents a simulation-based comparison of the proposed structure with other ACCUFET approaches, namely, planar and trench-gate ACCUFETs. As identical model parameters and simulation conditions are used, this comparison enables illustration and analysis of the inherent advantages and strengths of the ACCUFET structures themselves. The relevant technological

Fig. 1. Novel SiC ACCUFET structure.

issues, related to the considered ACCUFET approaches, are qualitatively discussed in Section IV-B.

II. DEVICE STRUCTURE AND OPERATION

The basic cell structure of the novel ACCUFET is shown in Fig. 1. In this structure, a thin N-channel surface epilayer is grown on the top of P-base epilayer, and a narrow trench is etched around each MOSFET cell. The trench region is ion-implanted to form the thin N-type region that acts as part of the drift region (path) for the conduction of electrons from the source to drain. At zero gate bias, there is no path for conduction of electrons because the top N-channel epilayer is completely depleted by the built-in fields, created by the P-base–N-channel epilayer junction and the gate electrode. This results in a normally-off device at zero gate bias with the drain voltage mostly supported by the N-drift region. When a positive gate bias is applied, an accumulation channel of electrons is created at SiO₂–SiC interface. This results in a low resistance path for the electron current, which flows from the source through the channel, then down to the drain through the trench and the drift region.

The main feature of this accumulation-type MOSFET is the N-type channel, epitaxially grown on P-base region. The two epilayers provide independent control of the doping concentration and thickness of the N-channel and P-base region. Therefore, by varying the thickness and doping concentration of these two epilayers, as well as the underlying N-drift region, a power MOSFET with optimum blocking voltage, on resistance, and threshold voltage can be designed. Another important feature relates to the fact that a planar MOS structure, created on high-quality epitaxial layer, is utilized with this approach. As a result,

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many of the open issues related to reliability of MOS interface in SiC can be addressed.

III. ANALYSIS AND OPTIMIZATION OF DEVICE PARAMETERS

Five parameters, characteristic of the new structure, are chosen to analyze the relationship between blocking and driving capability of the novel ACCUFET. These parameters are peak doping concentration of ion-implanted trench region, doping concentration and thickness of P-base epilayer, and doping concentration and thickness of N-channel epilayer.

A. Simulation Parameters and Models

Two-dimensional numerical-simulation structure (including the mesh, the boundaries, and the impurity profiles) for the device was generated in MEDICI [11], using all the 4H-SiC parameters provided in [12], [13]. As no detailed parameters for the impact ionization model have been reported for 4H SiC, the values reported for 6H SiC [14] were used in the simulation. Also, the analytical mobility model for concentration and temperature dependences, developed for silicon and gallium arsenide, was used with the maximum electron mobility set to $200 \text{ cm}^2/\text{Vs}$.¹ Moreover, as the carrier mobility is typically lower along the insulator–semiconductor interface than in the bulk of the semiconductor, a mobility degradation factor of 50% was used to account for this effect. This means that the actual channel carrier mobility was less than $100 \text{ cm}^2/\text{Vs}$, depending on the normal field and other factors. Due to symmetry of the device, only half of the device structure was evaluated. The simulated structure has a fixed $10\text{-}\mu\text{m}$ thick N-drift region doped at $1.0 \times 10^{16} \text{ cm}^{-3}$, an N^+ -type polysilicon gate electrode with an 80-nm thick gate oxide ($Q_F = 1.0 \times 10^{11} \text{ cm}^{-2}$), a channel length of $2.0 \mu\text{m}$, and a half cell pitch of $10 \mu\text{m}$.

The simulation results were used to calculate Baliga's figure of merit (BFOM) as the criterion for structure optimization and comparison. BFOM is given by [15]

$$\text{BFOM} = \frac{V_B^2}{R_{\text{ON}}}$$

where R_{ON} is the on-resistance and V_B is the maximum operating voltage which is set either by the avalanche-breakdown voltage, punchthrough voltage, or the drain-to-source voltage that corresponds to the maximum set oxide field (3 MV/cm in this paper).

B. Peak Trench Region Concentration

The first step in optimizing this MOSFET was to determine the peak trench region concentration that will provide optimum blocking capability and on-resistance of the device. Since the N-type trench region has to be formed by ion implantation into the P-base layer, i.e., the peak concentration of the ion-implanted trench region has to be set higher than the P-base background concentration (N_A), the background concentration

of the P-base epilayer has to be optimized accordingly. Three background concentrations of $6.0 \times 10^{16} \text{ cm}^{-3}$, $1.0 \times 10^{17} \text{ cm}^{-3}$, and $1.5 \times 10^{17} \text{ cm}^{-3}$ of $2.0\text{-}\mu\text{m}$ thick P-base epilayer were simulated, and the peak concentration of the ion-implanted region was varied from $6.3 \times 10^{16} \text{ cm}^{-3}$ to $9.0 \times 10^{16} \text{ cm}^{-3}$ for $N_A = 6.0 \times 10^{16} \text{ cm}^{-3}$, from $1.05 \times 10^{17} \text{ cm}^{-3}$ to $1.5 \times 10^{17} \text{ cm}^{-3}$ for $N_A = 1.0 \times 10^{17} \text{ cm}^{-3}$, and from $1.575 \times 10^{17} \text{ cm}^{-3}$ to $2.25 \times 10^{17} \text{ cm}^{-3}$ for $N_A = 1.5 \times 10^{17} \text{ cm}^{-3}$.

From the simulations results shown in Fig. 2, it was found that the maximum blocking voltage was achieved with $N_A = 1.0 \times 10^{17} \text{ cm}^{-3}$ and with a slightly higher peak trench region concentration of $1.05 \times 10^{17} \text{ cm}^{-3}$ (this value was used as the closest reasonable value to the P-base concentration of $1.0 \times 10^{17} \text{ cm}^{-3}$). The maximum operating voltage in this region (P-base concentration of $1.0 \times 10^{17} \text{ cm}^{-3}$) is determined by the maximum oxide field set at $E_{\text{OX}} = 3 \text{ MV/cm}$. An increase in the peak trench region concentration causes the maximum oxide field to occur at lower drain voltage. For the case of $N_A = 1.5 \times 10^{17} \text{ cm}^{-3}$, avalanche breakdown occurring in the trench region determines the blocking capability of the device. On the other hand, punchthrough breakdown determines the maximum operating voltage when the P-base background concentration is equal to $6.0 \times 10^{16} \text{ cm}^{-3}$. Although the N-channel epilayer is fully depleted in off mode, in the case of low N_A , the depletion-layer fields of the P-base–N-channel junction and the gate are not strong enough to shield the high electric field from the drain, resulting in punchthrough breakdown. In addition to that, the maximum oxide field increases as N_A is decreased, because the compensating effect of the built-in field is reduced.

To summarize, the peak concentration of the ion-implanted trench region strongly influences the maximum operating voltage of the device. To obtain the maximum operating voltage, the peak concentration of the ion-implanted trench region has to be slightly higher than the background concentration of the P-base epilayer. The concentration of the P-base epilayer itself cannot be set too low due to punchthrough breakdown and increasing oxide field, as the compensating effect of the built-in electric field is reduced.

However, it is not the maximum operating voltage alone, but rather the figure of merit (FOM) for power devices that is used to optimize the considered parameters. This involves the on-resistance of the device, which is decreased as the peak concentration of the trench region is increased. As Fig. 2 shows, the best trade-off between the breakdown voltage and on-resistance requirements in terms of BFOM is achieved with the peak trench region concentration of $1.4 \times 10^{17} \text{ cm}^{-3}$.

C. P-Base Layer Thickness

The thickness of the P-base epilayer is important, because it determines the depth/length of the trench region, which in turn affects the gate oxide field, breakdown voltage, and on-resistance. The effects of the P-base layer thickness (W_P) on maximum operating voltage, on-resistance, and BFOM of the device are shown in Fig. 3. In this simulation, the optimum values of the parameters considered in the previous section are used. With P-base concentration of $1.0 \times 10^{17} \text{ cm}^{-3}$ and peak trench region concentration of $1.4 \times 10^{17} \text{ cm}^{-3}$, punchthrough breakdown

¹It should be noted, however, that the contribution and the conclusions in this paper do not rely on quantitative results. The methodology used in the paper (simulation and comparison of ACCUFET approaches) focuses on the merits of the device structure itself, independent of the specific parameter values, which are still dominated by different technology imperfections.

Fig. 2. Effects of peak trench-region concentration (N_{peak}) on maximum operating voltage, on-resistance, and BFOM. $W_P = 2.0 \mu\text{m}$, $W_N = 0.4 \mu\text{m}$, $N_D = 1 \times 10^{16} \text{ cm}^{-3}$.

limits the thickness of the P-base epilayer to minimum value of $W_P = 1.2 \mu\text{m}$. On the other hand, avalanche breakdown determines the blocking capability of the device for $W_P \geq 2.2 \mu\text{m}$. The region of $1.2 \mu\text{m} \leq W_P \leq 2.2 \mu\text{m}$ is selected for detailed analysis and search for the optimum value (the region of $W_P \geq 2.2 \mu\text{m}$ is not of interest because the on-resistance increases rapidly due to increasing length of the trench region).

As shown in Fig. 3, an increase of the P-base thickness from $1.2 \mu\text{m}$ to $2.2 \mu\text{m}$, leads to increase of the maximum operating voltage from 500 V to just below 1700 V. The maximum electric field of 3 MV/cm in the oxide appears as the limit to the maximum operating voltage over this range of P-base thickness, except for the case of $W_P = 2.2 \mu\text{m}$ where its value is limited by the avalanche breakdown. The device on-resistance also increases over this range of P-base thickness. The graph in Fig. 3 shows that the P-base epilayer thickness of $2.0 \mu\text{m}$ is the optimum value in terms of BFOM.

D. Thickness and Concentration of N-Channel Epilayer

In this section, the effects of varying thickness (W_N) and doping concentration (N_{CH}) of the N-channel epilayer were investigated. The results are shown in Fig. 4. The dashed line indicates the punchthrough limit: the punchthrough current through the N-channel epilayer becomes too large when N_{CH} is increased beyond the dashed line for a given W_N . Left of the dashed line, the maximum gate oxide field (set at 3 MV/cm)

Fig. 3. Effects of P-base thickness (W_P) on maximum operating voltage, on-resistance, and BFOM. The difference between N_{peak} and P-base concentration is set to $4 \times 10^{16} \text{ cm}^{-3}$; $W_N = 0.4 \mu\text{m}$ and $N_D = 1 \times 10^{16} \text{ cm}^{-3}$, and $N_A = 1 \times 10^{17} \text{ cm}^{-3}$.

determines the maximum operating voltage with the exception of $W_N = 0.3 \mu\text{m}$ and high N_{CH} values, where the avalanche breakdown before the maximum gate oxide field is reached. Fig. 4 also shows the dependence of the on-resistance on W_N and N_{CH} . As can be observed, an increase in N_{CH} does not have much effect on the on-resistance, because majority of the current flows through the accumulation layer at the interface. Nonetheless, increasing W_N reduces the on-resistance, this being due to a decrease in the threshold voltage of the device. The maximum BFOM value of $6.3 \times 10^5 \text{ V}^2/\Omega$ is achieved with $0.5 \mu\text{m}$ thickness and $8.0 \times 10^{15} \text{ cm}^{-3}$ concentration of the N-channel epilayer.

Overall, the maximum BFOM value of the simulated device is achieved with $2.0\text{-}\mu\text{m}$ P-base epilayer doped at $1.0 \times 10^{17} \text{ cm}^{-3}$, ion-implanted trench region with peak concentration of $1.4 \times 10^{17} \text{ cm}^{-3}$, and N-channel epilayer concentration and thickness of $8.0 \times 10^{15} \text{ cm}^{-3}$ and $0.5 \mu\text{m}$, respectively.

IV. COMPARISON-BASED EVALUATION OF THE NOVEL STRUCTURE

In this section, the novel structure is compared to two alternative ACCUFET approaches, referred to henceforth as *trench-gate* and *planar*. The specific structures, selected to represent the trench-gate and the planar approaches, were published in [6] and [6]–[10], respectively. It should be emphasized

Fig. 4. Effects of N-channel concentration and thickness (W_N) on maximum operating voltage, on-resistance, and BFOM. $W_P = 2.0 \mu\text{m}$, $N_D = 1 \times 10^{16} \text{ cm}^{-3}$, $N_A = 1 \times 10^{17} \text{ cm}^{-3}$.

that the same models and parameters were used in the MEDICI device simulator to obtain and compare the performance characteristics of all the simulated structures.

A. Electrical Performance

The simulated structures of the alternative ACCUFETs are shown in Fig. 5. Due to symmetry of all the compared device structures, only half of the device cells are shown. The trench-gate structure has been extensively investigated and applied to 6H SiC [16]–[19]. Recent development in trench-gate ACCUFETs on 6H SiC demonstrated a device that is capable of withstanding voltage of 450 V with a low on-resistance of $23.84 \text{ m}\Omega \text{ cm}^2$ [6]. The design concept of the trench-gate approach is schematically illustrated in Fig. 5(a). The main feature of this structure is that the N-channel region is epitaxially grown on the trench sidewall to form the MOS structure. The electron current flows through accumulation channel formed at the trench sidewall, from the source toward the drain contact. The planar ACCUFET approach is illustrated in Fig. 5(b). In this structure, a thin N-type epilayer is grown epitaxially over a P^+ -type region, implanted into N-type drift layer. The ion-implanted P^+ buried region separates the thin epitaxially grown N-type and the thicker N-drift layer. The electron current flows laterally through the accumulation channel formed at the surface of top N-type region, and then

Fig. 5. Alternative ACCUFET structures: (a) trench-gate approach and (b) planar approach.

vertically toward the drain contact through the opening between the P^+ buried regions (JFET region). It has been shown that the optimized device has a $2.0\text{-}\mu\text{m}$ separation distance between the P^+ regions [7], [10]. The crucial device parameters that have been established in [6] and [10] for the trench-gate and planar structure approach, respectively, are used in this simulation and analysis.² However, in order to enable meaningful comparison, the common parameters are set to identical values: all of the compared structures are set to have a drift region thickness and concentration of $10 \mu\text{m}$ and $1.0 \times 10^{16} \text{ cm}^{-3}$ respectively, channel length of $2.0 \mu\text{m}$, an N^+ -type polysilicon gate electrode over an 80-nm thick gate oxide ($Q_F = 1.0 \times 10^{11} \text{ cm}^{-2}$), an N^+ region concentration of $1.0 \times 10^{20} \text{ cm}^{-3}$, and a Gaussian doping profile with characteristic width of $0.15 \mu\text{m}$ (where applicable). No other optimization was done in trench-gate and planar ACCUFET structures beyond those already performed in [6], [7], and [10], respectively.

²The thickness and impurity concentration of the trench-gate ACCUFET sidewall epilayer were $0.3 \mu\text{m}$ and $1 \times 10^{16} \text{ cm}^{-3}$, respectively [6]. The thickness and impurity of the planar ACCUFET P^+ -base implanted region were $0.5 \mu\text{m}$ and $1 \times 10^{20} \text{ cm}^{-3}$, respectively, and the thickness and impurity of the channel epilayer were $0.6 \mu\text{m}$ and $1.0 \times 10^{16} \text{ cm}^{-3}$, respectively [8].

Fig. 6. Comparison of simulated transfer characteristics.

TABLE I
COMPARISON OF ACCUFET STRUCTURES

Structure	On resistance (Ω) (@ $V_{GS}=5V$, $V_{DS}=1V$)	Max. Operating Voltage (V)	BFOM (V^2/Ω)
Novel	3.69	1530	6.3×10^5
Planar	5.23	1215	2.8×10^5
Trench-Gate	2.67	870	2.8×10^5

The obtained current–voltage characteristics for $V_{DS} = 1$ V are shown in Fig. 6, and they were used to calculate the on-resistances. Additional simulations were performed to obtain the maximum operating voltages, so that the BFOM could be calculated. The results for on-resistance, maximum operating voltage and BFOM are listed in Table I. The results show clearly that the new ACCUFET structure enables a BFOM value 2.25 higher than the trench-gate and the planar approaches.

Fundamentally, the trench-MOS device was proposed for its low on-resistance and relatively high blocking capability compared to other MOSFET devices [19]–[21]. As shown by the simulation results, the trench-gate ACCUFET has the smallest on-resistance, but also the lowest breakdown voltage as compared to the others. The major contribution to the on-resistance in the trench-gate structure comes from the channel resistance R_{CH} and the drift region-resistance R_{DRIFT} . In terms of the breakdown voltage, the avalanche breakdown limits its blocking capability, due to the localized high electric field near the trench base level.

Focusing on the planar device, let us note first that the thickness of P-base region is limited by the ion-implant process involved. Hence, to achieve a high blocking voltage, the P^+ region has to be implanted with a high dose. However, the high concentration of the P^+ region creates a high electric field in the depletion region across the P–N junction (JFET region), where the avalanche breakdown is more likely to occur. It should also be mentioned that this built-in potential plays a shielding role, reducing the electric field stress of the oxide and limiting the electron current in off mode. The distance between the P^+ regions determines the tradeoff between the on-resistance and the breakdown voltage. Small opening between the P-base regions results

in a device with high breakdown voltage and high on-resistance, while wider opening will result in lower breakdown voltage and lower on-resistance. A good tradeoff between these requirements was achieved with $2.0\text{-}\mu\text{m}$ separation distance of the buried P^+ region [7], [10]. As shown in Table I, the planar structure has a medium blocking voltage capability and the highest on-resistance. In the case of the novel structure, the peak concentration of ion-implanted trench region influences its performance in an analogous way to the separation distance of the JFET region in the planar device. The ion-implanted trench region determines the opening for the electron current path. The ability to control the thickness and concentration of the P-base epilayer in the novel device gives an advantage in terms of tailoring the device electrical performance. In calculating the on-resistance, the channel width was set to 10 μm for the novel ACCUFET structure. To compensate for the effect of a wider unit cell of the novel structure, the on-resistance of the trench and planar structures were reduced by the half-cell pitch ratio of 10.5:10.

B. Device Processing Considerations

The analysis and comparison presented in the previous section are focused on the device structures, and to distill the device-structure effects, any process-related differences are removed by selecting equal parameters for all the structures considered. This section addresses the main process-related effects in a descriptive manner.

A disadvantage of the trench structure is the fact that the gate oxide is grown on a sloped surface.³ It was shown that the problems could be alleviated by deposition of an epilayer on the etched surface [6], however, there are inherent problems with the sloped surface.

- 1) It was shown that epilayers grown on sloped surfaces exhibit terrace profile [22].
- 2) The defects from the reactive ion etching (RIE) used to create this surface could affect the quality of the epilayer [23]–[26].
- 3) Anisotropic oxidation rates [27] result in nonuniform oxide when grown on a sloped surface [28].

All these factors adversely affect the gate oxide and its interface with the SiC, in particular, in terms of the oxide reliability [19], [29], [30].

In the case of the planar ACCUFET approach, the P-base region is formed by high-dose ion implantation of boron, a process that may leave damage in the top $0.2\text{--}0.25\text{ }\mu\text{m}$ region from the surface [31]. The channel, epitaxially formed over the damaged region, would exhibit increased leakage current between the source and drain. The fact that the P^+ region is formed by ion implantation is also related to inability to independently control its thickness and doping. However, this effect is included in the simulation results presented in the previous section.

The quality of the channel region in the novel ACCUFET is not compromised by these process-related issues. The solution for the channel region offers not only more robust technology, but also additional comparative advantages in electrical performance, such as oxide reliability and channel carrier mobility.

³Although Fig. 5(a) shows this surface as vertical, in reality the angle is 70° [7].

To clarify this statement, it should be emphasized again that the simulation results given in the previous section are for identical technological parameters, including channel carrier mobility.

V. SUMMARY

The novel design structure of ACCUFET for high-power applications has been proposed. MEDICI device simulations were used to analyze the novel structure, as implemented in 4H SiC. The characteristic parameters (the peak trench region concentration, the thickness and concentration of the P-base layer, and the thickness and concentration of the N-channel epilayer) were analyzed in terms of their influences on the on-resistance and maximum operating voltage. The peak concentration of the ion-implanted trench region strongly influences the breakdown voltage and on-resistance of the device. Setting the peak concentration slightly higher than the background concentration of the P-base epilayer provides maximum operating/blocking voltage, however the on-resistance suffers due to low net carrier concentration in the trench region. On other hand, increasing the peak concentration of the trench region reduces the maximum operating voltage of the device. The doping concentration and the thickness of the P-base region are the most important design parameters for determining the blocking voltage and on-resistance of the novel device. Decreasing the P-base doping concentration below $1.0 \times 10^{17} \text{ cm}^{-3}$ decreases the blocking capability of the device due to the punchthrough in the P-base epilayer. On the other hand, the maximum operating voltage is limited by the maximum oxide field (set at 3 MV/cm), when the p-base concentration is increased to $1.0 \times 10^{17} \text{ cm}^{-3}$. If increased further, the maximum operating voltage becomes limited by the avalanche breakdown. The best tradeoff between these requirements is achieved by setting the P-base background concentration at $1.0 \times 10^{17} \text{ cm}^{-3}$, and the peak trench concentration at $1.4 \times 10^{17} \text{ cm}^{-3}$. Due to reasonably high net carrier concentration in the trench region, changing the thickness of the P-base epilayer does not change the on-resistance significantly. However, it does change the maximum operating/blocking voltage of the device. The maximum BFOM value was obtained with P-base thickness of 2.0 μm . The concentration of N-channel epilayer has the least effect on the on-resistance, due to the appearance of accumulation layer at the surface. However, its thickness has significant effect on the on-resistance (due to the shift in the threshold voltage) and on the maximum operating voltage (due to punchthrough in the channel).

The following optimum values have been established: channel thickness and concentration of 0.5 μm and $8.0 \times 10^{15} \text{ cm}^{-3}$, respectively, P-base epilayer thickness and concentration of 2.0 μm and $1.0 \times 10^{17} \text{ cm}^{-3}$, respectively, and trench region ion-implanted peak concentration of $1.4 \times 10^{17} \text{ cm}^{-3}$.

The simulation based evaluation of the novel ACCUFET included comparison to trench-gate and planar ACCUFETs, as representatives of two alternative approaches. Given that a number of ACCUFETs, based on the alternative approaches, were manufactured and the electrical characteristics were published, our simulation-based comparison could focus on the merits of each of the considered structures. Finally, relevant technological issues were considered in qualitative terms.

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