Design and Analysis of UHF Micropower CMOS DTMOST Rectifiers

Ying-Khai Teh, *Student Member, IEEE*, Faisal Mohd-Yasin, *Member, IEEE*, Florence Choong, Mamun Ibne Reaz, *Member, IEEE*, and Albert V. Kordesch, *Senior Member, IEEE*

Abstract—Design and analysis of ultrahigh-frequency (UHF) micropower rectifiers based on a diode-connected dynamic threshold MOSFET (DTMOST) is discussed. An analytical design model for DTMOST rectifiers is derived based on curve-fitted diode equation parameters. Several DTMOST six-stage charge-pump rectifiers were designed and fabricated using a CMOS 0.18- μm process with deep n-well isolation. Measured results verified the design model with average accuracy of 10.85% for an input power level between -4 and 0 dBm. At the same time, three other rectifiers based on various types of transistors were fabricated on the same chip. The measured results are compared with a Schottky diode solution.

Index Terms—CMOS analog circuits, integrated circuit modeling, rectifiers, ultrahigh-frequency (UHF) integrated circuits.

I. INTRODUCTION

THE application of radio frequency identification (RFID) is growing in momentum, particularly in the ultrahigh-frequency (UHF) band, due to its middle- to long-range communication ability. The ratification of global UHF passive RFID standard ISO-18000-6C has further stimulated the interests of many researchers to pursue research and development work on UHF power rectifiers (or charge pumps) at the microwatt level. In fact, micropower rectifiers are not only limited to RFID, but they are also useful in power-scavenging modules of wireless sensor applications [1].

In the ground work [2] on UHF micropower rectifiers, the authors had made two important contributions: 1) the first time demonstration of a Dickson charge pump as a UHF RF rectifier and 2) the implementation of such rectifier with a Schottky barrier diode (SBD) in a CMOS process. Since it appears that SBD-based charge pumps offer the best performance, a number of subsequent UHF RFID works adopted this solution [3]. However, the main limitation of SBD solutions is the CMOS process itself, which needs to be specially modified and SBD

optimized [4]. Hence, much effort is made to develop other CMOS solutions to circumvent the SBD problem that is encountered by most CMOS processes. Some of the other alternate solutions proposed include native transistor [5], [6], silicon-on-insulator wafer [7], threshold programming by analog memory [8], and special biasing circuitry [9].

This brief examines a simple alternate solution that does not involve complex circuitry or process change—a dynamic threshold MOSFET (DTMOST). One of the most elegant DTMOST solutions is accomplished by tying the transistor gate and the substrate together. In the earlier generations of the CMOS, which have a threshold voltage of 1 V or more, the DTMOST option did not seem to be appealing. However, as the feature size of the CMOS continues to shrink and the threshold voltage continues to scale down, the DTMOST is starting to show very good potential as the effective threshold voltage is now approaching the SBD turn-on voltage. The DTMOST has a low leakage current when reverse biased and a higher current drive (a lower threshold voltage due to the forward-bias body effect) when turned on.

In Section II, the common multistage Dickson charge-pump circuit is presented. Then, the device characteristics and construction of the DTMOST is analyzed. In Section III, our modeling technique for DTMOST rectifiers is proposed. The proposed design model is based on the modified Bessel function solution derived from the classic exponential diode equation [10]. In Section IV, simulated results of the design model are compared with the measured performance of a test chip fabricated using a standard CMOS 0.18- μm process. In addition, rectifiers based on a native transistor were fabricated on the same die, and their performance was compared to the DTMOST rectifier. Section V contains concluding comments on observed design issues with design recommendations.

II. ANALYSIS OF THE RECTIFIER AND DTMOST DEVICE

Fig. 1 shows the N -stage Dickson charge-pump circuit, which is one of the most popular topologies used in UHF micropower rectifiers. The diode elements in Fig. 1 can be replaced with any diodelike rectifying device such as the SBD, p-n junction diode, or diode-connected MOST.

Circuit analytical modeling is only possible under a steady-state condition due to complications related to the initial transient behavior. The original output voltage equation published in [2] states that the output of this circuit is simply $N \times (V_{\text{RF}} - V_D)$, where V_{RF} is amplitude of the RF input signal, and V_D is the forward voltage of the diode element.

Manuscript received May 2, 2008; revised July 28, 2008 and October 15, 2008. Current version published February 25, 2009. This paper was recommended by Associate Editor M. Ghovanloo.

Y.-K. Teh and F. Mohd-Yasin are with the Faculty of Engineering, Multimedia University, 63100 Cyberjaya, Malaysia (e-mail: ykteh@mmu.edu.my).

F. Choong was with the Faculty of Engineering, Multimedia University, 63100 Cyberjaya, Malaysia. She is now with the Faculty of Engineering and Science, University of Tunku Abdul Rahman, 53300 Kuala Lumpur, Malaysia.

M. I. Reaz is with the Department of Electrical, Electronic and Systems Engineering, National University of Malaysia, 43600 Bangi, Malaysia.

A. V. Kordesch is with the Device Modeling Department, Silterra Malaysia, 09000 Kulim, Malaysia.

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/TCSII.2008.2010190

Fig. 1. N -stage Dickson charge-pump rectifier.

Fig. 2. DTMOST realized in an isolated deep n-well.

This equation is oversimplified due to two reasons. First, it assumes a diode to have a constant V_D . In a UHF RF rectifier application, the operating point is often at the microampere level. Hence, the diode forward voltage becomes a sensitive function of conducting current [11]. Second, this equation assumes the input signal to be approximately a square pulse, due to its historical usage in the nonvolatile memory charge pump. However, in a UHF RF micropower rectifier application, the input signal is actually a sinusoidal wave.

Hence, a number of recently reported works have proposed several formulas to model the Dickson charge-pump circuit under the UHF RF rectifying operation [6], [7], [10], [11]. For example, in [6], the authors provided a comprehensive model with an appropriate approximation of the BSIM3 model for MOST devices. It takes account of reverse leakage, conductance angle, and nonlinearity in the threshold voltage. Vita and Iannaccone [10] proposed a modified Bessel function solution, which is targeted at a diode-based charge pump and included the threshold nonlinearity effect. Barnett [11] modified the original Dickson equation to include all nonideality effects, as well as integrated impedance matching analysis. Finally, the model in [7] is based on numerical simulation alone and provides the most accurate results, with the shortcoming that it does not provide too much design insight.

In most CMOS processes, the DTMOST can be realized using a PMOS in a stand-alone n-well. However, in this brief, we choose to implement the DTMOST using deep n-well isolation, as shown in Fig. 2, for three reasons. First, a deep n-well provides better isolation of the DTMOST device, thus minimizing the noise level that could be coupled from nearby subcircuits [12]. Second, better device isolation alleviates a

Fig. 3. Equivalent circuit of a diode-connected DTMOST.

potential latch-up problem. Third, an NMOS in a deep n-well offers reduction of the gate capacitance C_G and higher intrinsic charge mobility relative to the PMOS, resulting in higher F_t and F_{max} [13]. Therefore, a deep n-well DTMOST rectifier is intrinsically able to work at a higher frequency region than a PMOS rectifier designed in a standard n-well. Moreover, for the same current driving strength, NMOS realizations usually require a smaller transistor size compared to their PMOS counterparts.

The effect of series resistance in the device can be ignored, since micropower UHF RF rectifying circuits operate under very low currents. The equivalent circuit of the DTMOST diode then becomes a parallel combination of three devices, namely, the transistor M_D , the diode D_{BS} , and the capacitance C_D (Fig. 3). The transistor M_D is a drain-gate connected MOSFET with a typical threshold voltage. The diode D_{BS} refers to the parasitic source-bulk p-n junction diode. Finally, the capacitance C_D represents a voltage-dependent lumped capacitance; it comprises the sum of the gate-source capacitance C_{GS} and the source-bulk diffusion capacitance C_{SB} . Due to the connection between the gate, drain, and bulk terminals, the other MOSFET capacitances (C_{GD} , C_{DB} , and C_{GB}) become insignificant. The gate-source capacitance C_{GS} has two components: 1) the overlap capacitance C_{GSO} and 2) the gate-to-channel capacitance C_{GCS} . Assuming that W and L are the drawn transistor gate width and length, respectively, C_{GSO} is simply $C_{OX} \times \Delta L \times W$. C_{OX} is the gate oxide capacitance, ΔL is the difference of the drawn gate length and effective gate length. C_{GCS} can be approximated using the following relation: $C_{OX} \times W \times L$ [14].

Under normal operating conditions of the MOST, the source-bulk capacitance is never forward biased. However, when the forward voltage of the DTMOST diode exceeds 0.6 V, the forward junction capacitance C_{SB} of the source-bulk junction diode will exponentially increase. The value of C_{SB} is given by the following standard abrupt junction capacitance formula:

$$C_{SB} = \frac{C_{jo}(L_S \times W_S)}{\left(1 - \frac{V_D}{V_{\gamma J}}\right)^{mj}} + \frac{C_{jsw}(2L_S + W_S)}{\left(1 - \frac{V_D}{V_{\gamma Jsw}}\right)^{mjsw}} \quad (1)$$

where C_{jo} is the zero-bias junction capacitance per unit area; C_{jsw} is the zero-bias sidewall capacitance per unit perimeter; L_S and W_S are the drawn source junction length and width, respectively; mj and $mjsw$ are the grading coefficients, which

Fig. 4. I – V characteristics of diode-connected conventional configured and DTMOST configured for typical V_{TH} transistors, and its curve-fit parameters.

values range from 0.4 to 0.5; $V_{\gamma J}$ and $V_{\gamma JSW}$ are the junction built-in voltages; and V_D is the applied input voltage. All the parameters are directly taken from the foundry BSIM3 models. It has to be noted that (1) is a simple capacitance model for designers to estimate a ballpark value. Equation (1) does not take into account the transit time–charge effect introduced by the diode/bipolar junction transistor compact model.

III. MODELING METHODOLOGIES

Extraction of the current–voltage (I – V) characteristics of DTMOST transistors can be done either from SPICE simulation or from actual device measurement. The measured I – V characteristics of a fabricated MOST device, with a width–length ratio of $10 \mu\text{m}/0.5 \mu\text{m}$, both in the conventional configuration (body tied to the ground) and DTMOST connection are shown in Fig. 4. In a $0.18\text{-}\mu\text{m}$ CMOS process, the turn-on voltage for the conventional configuration MOST is typically 0.45 V, whereas the DTMOST threshold voltage has shifted to 0.35 V. At a reverse-bias condition, the DTMOST configured transistor is off, and leakage has two components, namely, reverse diode leakage and subthreshold leakage.

Under the DTMOST connection, the device actually becomes a hybrid combination of the p–n diode and diode-connected MOST. By applying curve fitting upon the extracted I – V data, it can be shown that the DTMOST behavior is closer to a diode. At higher forward voltages, the DTMOST drain current approaches the exponential behavior rather than the square-law behavior because of the diode forward-bias action in the D_{BS} diode.

Hence, we choose to model the DTMOST diode I – V to emulate the classical diode equation, similar to the work in [10], and to add a nonideality factor η into the diode equation. To begin, first, the DTMOST I – V behavior is modeled as a diode, i.e.,

$$I_D \cong I_S \exp(V_D/\eta \cdot V_T) \quad (2)$$

where V_D is the applied diode voltage, and V_T is the thermal voltage. Application of curve fitting (2) upon the extracted I – V

data yields empirical values of the diode saturation current I_S and the nonideality factor η . The I – V characteristics of the DTMOST that is curve fitted to (2) are shown in Fig. 4. Fitting parameters I_S and η are chosen to have values of 1.261×10^{-7} and 2.992, respectively, which is a compromise that fits better for a higher diode voltage range (0.4–0.6 V).

After taking into account the factor η , the complete current equation of each DTMOST diode (which is also the rectifier output current) [10], inclusive of both ac and dc current components in the rectifier circuit in Fig. 1, is updated to

$$I_d = I_S \left[\exp \left(\pm \frac{V_o}{\eta V_T} \cos(\omega_o t) \right) \exp \left(-\frac{V_{out}}{2\eta N V_T} \right) - 1 \right] + C_D(V_D) \frac{dV_D}{dt} \quad (3)$$

where N is the number of stages of circuit in Fig. 1, V_{out} is the dc output voltage of the rectifier, ω_o is the RF carrier frequency in radians, and V_o is the amplitude of the RF input signal. Since this brief is interested in extracting the dc current component only, the frequency terms (ω_o) and capacitance current terms in (3) can be neglected. Subsequently, via the modified Bessel function series expansion [10], the diode dc current equation is now simplified to

$$I_{out} = I_S \left[B_0 \left(\frac{V_o}{\eta V_T} \right) \exp \left(-\frac{V_{out}}{2\eta N V_T} \right) - 1 \right]. \quad (4)$$

A general N -stage rectifier input–output relationship can be solved as follows:

$$\left(1 + \frac{I_{out}}{I_S} \right) \exp \left(\frac{V_{out}}{2\eta N V_T} \right) = B_0 \left(\frac{V_o}{\eta V_T} \right). \quad (5)$$

Designers can choose either I_{out} or V_{out} as the objective output parameter for the rectifier, leaving the other as a dependent variable. Both V_{out} and I_{out} are related by Ohm's law, which states that $V_{out} = I_{out} \times R_{load}$.

A. Parasitic Capacitance and Input Impedance Analysis

As mentioned in Section II, a forward-biased DTMOST diode has a large junction capacitance. The large capacitance eventually shunts away the RF power and lowers the effective RF voltage drop across the DTMOST diode. The effective RF voltage drop is determined by the ratio $C/(C + C_{parasitics})$. The capacitance C is the coupling charging capacitor. The parasitic capacitance $C_{parasitics}$ is found as the summation of all unwanted stray capacitances, such as the MOST capacitance (C_{GS} , C_{SB}) and substrate coupling capacitance (as extracted from foundry design manuals, with a typical value of several tens of femtofarads), in addition to the charging capacitor C . Although C_{SB} is a voltage-dependent parameter as suggested in (1), this brief takes only the worst-case value (highest capacitance possible) based on (1). C_{SB} is first calculated using the assumed incident RF input amplitude V_o from (1). The worst-case value for C_{SB} is calculated to be around 40 fF. To include

this capacitive division effect, V_o in (4) and (5) is updated as V'_o , i.e.,

$$V'_o = \frac{C}{C + C_{\text{parasitics}}} \times V_o. \quad (6)$$

After neglecting the substrate loss, the average input power P_{IN} can be found by taking the sum of the average power consumed by each diode P_D and the load power. P_D can be obtained by first calculating the integral of the diode voltage ($\pm V_o \cos(\omega_o t) - V_{\text{out}}/2N$) times the diode current in (3) and then dividing the integral by the period of one RF cycle. By taking into account the modified Bessel functions' mathematical properties, it can be found that

$$P_D = I_S V_o B_1 \left(\frac{V_o}{\eta V_T} \right) \exp \left(-\frac{V_{\text{out}}}{2\eta N V_T} \right) - \frac{V_{\text{out}} \times I_{\text{out}}}{2N} \quad (7)$$

and then P_{IN} can be calculated using (7), i.e.,

$$\begin{aligned} P_{\text{IN}} &= 2NP_D + V_{\text{out}} \times I_{\text{out}} \\ &= 2NI_S V_o B_1 \left(\frac{V_o}{\eta V_T} \right) \exp \left(-\frac{V_{\text{out}}}{2\eta N V_T} \right). \end{aligned} \quad (8)$$

For impedance matching, it is necessary to find the input impedance of the rectifier, which is a parallel combination of the equivalent resistance R_{eq} and capacitance C_{eq} , where

$$R_{\text{eq}} = V_o / 2NI_S B_1 \left(\frac{V_o}{\eta V_T} \right) \exp \left(-\frac{V_{\text{out}}}{2\eta N V_T} \right) \quad (9)$$

$$C_{\text{eq}} = \frac{N}{V_o} \int_{V_{D_{\min}}}^{V_{D_{\max}}} C_D(V_D) dV_D. \quad (10)$$

In (10), the diode capacitance C_D is the sum of C_{GS} and C_{SB} . The integration limits $V_{D_{\max}}$ and $V_{D_{\min}}$ (which are the maximum and minimum voltage drops across a single diode) have values of $(V_o - V_{\text{out}}/2N)$ and $(-V_o - V_{\text{out}}/2N)$, respectively.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

Four six-stage rectifiers were designed and fabricated using an industry standard CMOS 0.18- μm triple-well process. The test chip contains four rectifiers employing both standard V_{TH} thin-oxide and native (zero-threshold voltage) transistors, with each type of transistor configured in both the conventional connection (body tied to the circuit ground) and DTMOST connection (body tied to the gate). All transistors have a width-length ratio of 10 $\mu\text{m}/0.5 \mu\text{m}$. Each transistor is contained within its own individual deep n-well. The coupling capacitor size is 1 pF, and it is built using a metal-in-metal, which has high a Q -factor, a high capacitance density, and a low substrate loss. The total active area of a single rectifier is 0.06 mm^2 (including bonding pads), whereas the total test chip die size is 1 mm^2 . The bare dice are packaged in a SOIC-14 package. The chip micrograph is shown in Fig. 5.

A continuous-wave RF at 900 MHz with power swept from -7 to 0 dBm is injected into the rectifier input port via an SMA

Fig. 5. Rectifiers test chip micrograph.

Fig. 6. Rectifier test setup.

connection. The details of the measurement procedure can be found in [3] and [15]. It should be noted that in the absence of a properly designed matching network, the measured results are less than the optimum for the given circuit.

During the measurement process, a variable resistor is added to the rectifier output port to emulate an output load. Due to the sensitivity of the output voltage to the loaded impedance, the dc output voltage is measured via a discrete high-accuracy operational amplifier as a unity gain buffer in order to avoid the loading effect of a voltmeter. The rectifier in [3] has the same six-stage Dickson charge-pump topology using the SBD. In order to achieve a fair comparison with [3], the experiment setup is similar to [3], as shown in Fig. 6.

The measured experimental results are shown in Fig. 7, with measurement results from [3] included for comparison. The output resistor load of all rectifiers is set to 1 $\text{M}\Omega$, which is adjusted using the variable resistor. This setup implies that a 1-V output voltage will give a 1- μA output current. In general, all MOST-based circuits have worse performance than SBD-based circuits. The accuracy of this model is very poor at a low power level, i.e., up to a 100% mismatch is observed at -7 dBm. However, the measured output voltage of the DTMOST rectifier well matches the simulation model at a power level larger than -5 dBm. Accuracy of the model at -4 dBm is 21.7%, and it significantly improves as the power level rises. Finally, at 0 dBm, this model achieved accuracy of 3.75%. Average accuracy is 10.85% for power levels from -4 to 0 dBm. The power efficiency ($V_{\text{out}} \times I_{\text{out}}/\text{input power}$) of the circuit is dependent on the input RF amplitude level, which is strongly dependent on the antenna radiation impedance and impedance matching network [7].

Although not as good as the SBD, the measured performance of the DTMOST rectifier demonstrated that the DTMOST

Fig. 7. Measured and simulation results of various six-stage voltage multipliers as a function of the chip input power; the output resistive load is set to 1 M Ω .

rectifier is actually sufficient for applications that require a lower power sensitivity, for example, a UHF RFID that requires a short reading range (less than 3 m). As technology scales, the DTMOST rectifier performance is foreseen to approach the SBD solution. Hence, a DTMOST solution could be implemented on a new CMOS process where an SBD device is not available.

For a typical V_{TH} transistor, the DTMOST configuration has dramatically improved the rectifier's performance compared to conventionally configured transistors. However, the extra performance gain provided by the DTMOST technique does not apply to native transistors. Rectifiers built using DTMOST configured native transistors and conventional configured native transistors yield almost identical performance. This result experimentally validated the weak body effect of the native transistor argument in [6].

Many designers believe that the lower the threshold voltage of the MOSFET devices, the better the performance of the rectifiers. In contrast to this common belief, the companion rectifiers built from native transistors in this test chip demonstrated the poorest performance. This is due to the high leakage current during the reverse RF cycle, as suggested in [9]. Occasionally, near-zero threshold voltage transistors could cause potential issues due to the process fluctuation that results in an excessive leakage current up to the microampere level (which is significant in a UHF RF rectifier application). In this perspective, a DTMOST configured typical V_{TH} transistor has an advantage over the native transistor as typical V_{TH} transistors usually have stable and foundry-optimized process parameters (a controlled leakage current level).

V. CONCLUSION

The design and modeling of UHF micropower CMOS DTMOST rectifiers has been presented. An analytical model

was derived based on the diode equation with a nonideality factor curve fitted to experimentally obtained $I-V$ data. Actual measurement from fabricated chips validated the proposed analytical model and proved the feasibility of the DTMOST solution. In conclusion, the DTMOST realized with a deep n-well process is a promising alternate solution for CMOS processes where the SBD is not available.

ACKNOWLEDGMENT

The authors would like to thank Silterra Malaysia for chip fabrication, Emerald Systems for chip packaging, and Dr. R. Sobot from The University of Western Ontario, London, ON, Canada, for his thoughtful feedback and comments on this brief.

REFERENCES

- [1] B. C. Yen and J. H. Lang, "A variable-capacitance vibration-to-electric energy harvester," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 2, pp. 288–295, Feb. 2006.
- [2] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7- μ W minimum RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1602–1608, Oct. 2003.
- [3] N. Tran, B. Lee, and J. W. Lee, "Development of long-range UHF-band RFID tag chip using Schottky diodes in standard CMOS technology," in *Proc. IEEE RFIC Symp.*, Jun. 3–5, 2007, pp. 281–284.
- [4] W. C. Jeon, T. M. Fireston, J. C. Rodgers, and J. Melngailis, "Design and fabrication of Schottky diode, on-chip RF power detector," *Solid State Electron.*, vol. 48, no. 10/11, pp. 2089–2093, Oct. 2004.
- [5] Y. Yao, Y. Shi, and F. F. Dai, "A novel low-power input-independent MOS AC/DC charge pump," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2005, pp. 380–383.
- [6] J. Yi, W. H. Ki, and C. Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 1, pp. 153–166, Jan. 2007.
- [7] J. P. Curty, N. Joehl, F. Krummenacher, C. Dehollain, and M. J. Declercq, "A model for μ -power rectifier analysis and design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2771–2779, Dec. 2005.
- [8] R. Glidde and J. Schroeter, "Bringing long-range UHF RFID tags into mainstream supply chain applications," *RF Des. Mag.*, vol. 28, no. 7, pp. 24–30, Jul. 2005.
- [9] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35–41, Jan. 2006.
- [10] G. D. Vita and G. Iannaccone, "Design criteria for the RF section of UHF and microwave passive RFID transponders," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 9, pp. 2978–2990, Sep. 2005.
- [11] R. E. Barnett, "High efficiency RF to DC conversion and ultra-low-power analog front end circuits for low-cost field-powered UHF RFID," Ph.D. dissertation, Dept. Elect. Eng., Univ. Texas at Dallas, Richardson, TX, Dec. 2007.
- [12] C. Y. Chang, J. G. Su, H. M. Hsu, S. C. Wong, T. Y. Huang, and Y. C. Sun, "Investigations of bulk dynamic threshold-voltage MOSFET with 65 GHz "normal-mode" f_t and 220 GHz "over-drive mode" f_t for RF applications," in *VLSI Symp. Tech. Dig.*, Jun. 2001, pp. 89–90.
- [13] J. G. Su, H. M. Hsu, S. C. Wong, C. Y. Chang, T. Y. Huang, and Y. C. Sun, "Improving the RF performance of 0.18 μ m CMOS with deep n-well implantation," *IEEE Electron Device Lett.*, vol. 22, no. 10, pp. 481–483, Oct. 2001.
- [14] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ: Pearson Educ. Int., 2003, pp. 107–112.
- [15] A. Facen and A. Boni, "CMOS power retriever for UHF RFID tags," *Electron. Lett.*, vol. 43, no. 25, pp. 1424–1425, Dec. 6, 2007.