Investigation of Ultralow Leakage in MOS Capacitors on 4H SiC

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Abstract—Ultralow leakage current through nitrided gate oxides on 4H SiC is investigated by a novel technique in this paper. The technique utilizes capacitance–voltage (C – V) measurements to characterize the relaxation of nonequilibrium capacitance due to charge leakage in floating-gate metal–oxide–semiconductor capacitors. The C – V measurements are performed at elevated temperatures and the results are extrapolated to room temperature. The obtained values for the relaxation times are in the order of 10^{13} s for MOS capacitors on both n-type and p-type 4H SiC.

Index Terms—Nitrided gate oxides, nonvolatile memories, silicon carbide, ultralow leakage.

I. INTRODUCTION

NITRIDED GATE oxides provide industrial-standard electronic passivation of the SiC surface, enabling development of commercial metal–oxide–semiconductor (MOS) devices [1]–[9]. One of the applications of MOS devices on SiC is for nonvolatile random-access memories (NVRAMs) [10]–[18]. Given that the volatile characteristics of Si-based DRAMs are due to several severe leakage paths [19], [20], experimental investigations of these leakage mechanisms in SiC is necessary for the development and design of SiC-based NVRAMs.

One of the leakage mechanisms that has been extensively investigated and reported is due to electron-hole generation in the depletion region of an SiC-based MOS capacitor [11], [12], [14]–[18]. The estimated relaxation times of capacitance recovery from deep-depletion to inversion levels at room temperature are 10^{17} s and 10^{13} s for n-type 4H and 6H SiC, respectively, [14]–[17]. A somewhat shorter capacitance-recovery time has been demonstrated by MOS capacitors on p-type 4H SiC [18]. Nonetheless, these times are so long that any leakage due to surface carrier generation can be neglected when developing and designing SiC-based NVRAMs.

Another leakage path is through the gate-dielectric of a MOS capacitor. The importance of this leakage mechanism has been experimentally demonstrated for MOS capacitors on 4H SiC with dry oxide [14]. The relatively high leakage current in these samples has been attributed to the poor quality of the oxide. Using gate oxides processed by nitridation, the leakage current

Fig. 1. Typical high-frequency C – V curves, measured before and after UV illumination at the point of maximum inversion bias. The arrows indicate sweeping direction.

through the gate oxide is significantly reduced [14], most likely due to significant reduction of carbon clusters at the nitrided SiC–SiO₂ interfaces [21], [22]. Importantly, there has not been any quantitative measurement of the gate-oxide leakage. This is because the leakage current through the gate oxide can be many orders of magnitude lower than the current corresponding to the flow of one electron per second, so it is practically impossible to measure it directly. In this paper, a novel measurement technique for characterization of the loss of nonequilibrium charge due to ultralow gate-oxide leakage is proposed and demonstrated for the case of MOS capacitors on both n-type and p-type 4H SiC substrates.

II. EXPERIMENTAL DETAILS

Manufactured by CREE Research, 4H-SiC wafers were used to fabricate MOS structures. Nitrided gate oxides 30–38 nm thick were grown on the wafers using the sandwich technique (nitridation–oxidation–nitridation). The sandwich technique was selected because it provides high-quality oxides with minimized use of nitric oxide and minimized growth time. More details on the sandwich technique and the associated processing of MOS capacitors is provided elsewhere [5].

Fig. 1 shows typical high-frequency (100 kHz) C – V curves for both types of MOS capacitors. Constant capacitance levels, well above the theoretical inversion levels, are observed with both types of capacitors when measuring from deep-depletion toward accumulation after illumination with UV light. These constant capacitance levels indicate that excess minority carriers is generated by the UV light and that this nonequilibrium

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Fig. 2. C - t plot for an n-type MOS capacitor, measured at 300 °C, as an illustration of the floating-gate technique.

charge is retained in the potential well created by the surface band bending for gate voltages that corresponds to the inversion region. Unlike the n-type MOS capacitors, an “interface-state ledge” is observed in the C - V curves of p-type MOS capacitors. This ledge is attributed to the capturing of electrons at the SiC-SiO₂ interface, implying that the interface trap density is higher in the lower half of the energy gap. This conclusion is consistent with the interface-trap densities of MOS capacitors on n-type and p-type substrates measured by the conductance technique [16], [18].

III. DESCRIPTION OF THE FLOATING-GATE TECHNIQUE

Due to extremely slow thermal generation in SiC, even at temperatures as high as 300 °C, UV light was used to generate minority carriers. To set an MOS capacitor in the inversion state, the gate was biased so that the minority carriers generated by the UV light are attracted to the semiconductor surface. Capacitance-transient (C - t) measurements were used to detect the changes at the semiconductor surface by a computer-controlled HP4284A LCR meter. Being a source of external carrier generation, the UV light leads to a capacitance increase that is well above the theoretical inversion level if the light intensity is sufficient. This is illustrated in Fig. 2 for the case of a MOS capacitor on n-type 4H SiC. The deep-depletion and inversion levels indicated on the figure have been determined by a standard method described elsewhere [14]–[16].

An increase in high-frequency (HF) capacitance is directly related to a corresponding decrease in the depletion layer width (w_d). The energy-band diagrams in Fig. 3 illustrate the changes of the depletion layer width of n-type MOS capacitors in: 1) deep depletion; 2) above-inversion; and 3) equilibrium state of strong inversion. For as long as the capacitance increases from the deep-depletion to above-inversion levels, the depletion-layer width continues to decrease because the positive charge of the donor ions in the depletion layer is replaced by increasing density of minority holes. The capacitance increase saturates at a certain level that corresponds to equal rates of external hole generation (the thermal-generation rate is negligible) and hole

Fig. 3. Energy-band diagrams of an n-type MOS capacitor biased in inversion at different conditions. (a) Deep depletion (a nonequilibrium condition). (b) Above inversion with UV light exposure (a steady-state nonequilibrium condition). (c) Inversion (the thermal-equilibrium condition). The depletion-layer width w_d relates to the HF capacitance.

removal by recombination, emission into the substrate, and/or gate-oxide leakage.

Once this steady-state capacitance level is reached, the UV light is turned off to remove the source of external carrier generation. As the carrier-recombination rate is no longer balanced by the external-generation rate, excess minority carriers are recombined and the capacitance drops toward the inversion level. As Fig. 2 shows, the capacitance can remain at the strong-inversion level if the thermal generation is strong enough to compensate for any loss of holes due to leakage through the gate oxide—just as is the case in silicon. The thermal generation and the oxide leakage are two competing mechanisms because the thermal generation works to maintain the equilibrium state in the semiconductor, whereas the oxide leakage works toward establishing equilibrium condition across the MOS capacitor (be-

tween the gate electrode and the semiconductor). If the oxide leakage current is too high, or the thermal generation is too low (such as in SiC at room temperature [11], [12], [14]–[18]), the loss of holes due to oxide leakage would not be compensated and the capacitance decay would cross the inversion level [14].

The described procedure of setting the MOS capacitor in strong inversion has been used to just prepare the structure for the beginning of the ultralow leakage measurements. The aim is to start measuring the leakage from a well defined reference point, which correspond to a thermal-equilibrium condition in the semiconductor but sets a nonequilibrium condition across the gate oxide—the capacitor is charged to the level of strong inversion. Therefore the leakage measurements begin at the point when the gate is set in floating mode by disconnecting the probe that connects the gate voltage.

Once set in floating mode, the leakage through the oxide removes both holes from the semiconductor and electrons from the metal electrode. This leads to a reduction in voltage across the oxide, but importantly, there is no need to generate new holes in order to maintain the equilibrium state in the semiconductor. Therefore, the gate-oxide leakage leads to a continuous reduction in the inversion-layer charge, as it works toward discharging the capacitor to remove the voltage difference between the gate and the semiconductor surface. As is well established, capacitance measurements of a fully discharged capacitor show the deep-depletion capacitance. This is because no holes can be generated to respond to the inversion-level voltage, so the surface is depleted to provide positive charge from the donor ions in the depletion layer. The important question here is what happens if a capacitance measurement, with the inversion-level gate voltage, is taken before the capacitor is fully discharged. The answer to this question is that the depletion layer is extended by the applied voltage to provide positive-donor ions that compensate for the holes that leaked away from the inversion layer. Therefore, the capacitance will be reduced below the inversion level, but for as long as there are some excess holes in the inversion layer, the capacitance will remain higher than the deep-depletion level.

The experimental results shown in Fig. 2 illustrate the capacitance reduction due to oxide leakage of a charged capacitor with floating gate. The capacitance measurements were performed by simply reconnecting the gate electrode to the original inversion-level voltage for a short time, needed to record the HF capacitance measurement. After the measurement is completed, the gate electrode is disconnected again until the next measurement.

It was found that the capacitance decay from the inversion toward the deep-depletion levels could be approximated by the following exponential equation:

$$C = C_{inv} + \Delta C \left[\exp \left(\frac{-t}{\tau} \right) \right] \quad (1)$$

where C is the variable capacitance, t is the time, ΔC is the difference between the inversion and the deep-depletion capacitance levels ($\Delta C = C_{inv} - C_{dd}$), and τ is the time constant. This time constant represents the capacitance-relaxation time at

TABLE I
ESTIMATED RELAXATION TIMES AT ROOM TEMPERATURE

N type	P type	
	No Shielding Ring	With shielding Ring
8×10^{12} s	2×10^{13} s	3×10^{12} s

the specific measurement temperature. Assuming exponential dependence of the relaxation time on temperature

$$\tau = B \exp \left(-\frac{E_A}{kT} \right) \quad (2)$$

where B is a constant and E_A is the process activation energy, the room-temperature value of τ and E_A can be estimated from the corresponding Arrhenius plot.

It should be noted that the described technique is not suitable for leakages through the oxide that are high enough to cause unmeasurably short discharge times. In such cases, however, direct current measurements may be possible. This technique is also not practical in the cases when the generation rate is so high that it would generate minority carriers during the short intervals when the gate voltage is applied to enable the capacitance measurements.

IV. RESULTS AND DISCUSSION

MOS capacitors with NO-nitrided gate oxides on both n-type and p-type 4H SiC were used in the experiment. The measurements were performed at temperatures ranging from 265 °C to 330 °C. The MOS capacitors were initially biased in accumulation and then instantaneously stepped to the set inversion-level voltage ($V_G = -5$ V and $V_G = 3$ V for the MOS capacitors on n-type and p-type substrates, respectively).

The measurements on the p-type substrate were performed in two ways: 1) without any shielding and 2) with a shielding ring biased at -5 V. It has been observed that the surface of p-type 4H SiC, surrounding a MOS capacitor, can be inverted even when the gate is grounded (thermal equilibrium) [18]. Consequently, any in-flow of minority electrons from the perimeter into the inversion layer under the gate would influence the measured relaxation time. This supply of electrons would act to replace some of the electrons lost by the gate oxide leakage, leading to longer relaxation times and impression of lower gate-oxide leakage (Table I). To remove this possible supply of electrons, measurements were also performed with capacitors having shielding rings that were biased at -5 V. The shielding rings were created at the same metal level as the gate metallization and were separated by 15- μ m gaps from each gate.

Fig. 4 shows typical capacitance-transient measurements obtained with capacitors on n-type [Fig. 4(a)] and p-type substrates for the case of shielded MOS capacitors [Fig. 4(b)]. The symbols are the experimental data whereas the lines show the fitting by (1). The relaxation times that provide the best fit are shown

Fig. 4. High-temperature plots at different temperatures measured with MOS capacitors on (a) n-type and (b) p-type 4H SiC substrates. The symbols are the measured data and the solid lines are the best fitting by (1).

Fig. 5. Arrhenius plots of the relaxation time measured with MOS capacitors on n-type and p-type 4H SiC substrates. The coefficients of determination r^2 are shown for each plot.

in Fig. 5. From the Arrhenius plots, shown in Fig. 5, room-temperature values were extracted and they are shown in Table I.

As can be seen, the relaxation times for nonshielded capacitors on p-type substrate were longer compared to the shielded

capacitors. This result shows that the effect of electron supply from the capacitor perimeter does exist. Comparing the results of shielded capacitors on p-type substrate to n-type substrate, we find no significant difference, within the measurement uncertainty. Importantly, the relaxation times in either case are very long, which points out to extremely low leakage currents. Nonetheless, these relaxation times are many orders of magnitude shorter than the published relaxation times associated with the generation process [14]–[18]. This shows that the leakage through the gate oxide is many orders of magnitude higher than any leakage current due to carrier generation.

V. CONCLUSION

In this paper, we have reported the first results on characterization of ultralow leakage through the gate oxides of MOS capacitors on n- and p-type 4H SiC. A novel technique, utilizing C - t measurements and floating gates, has been demonstrated as a simple characterization tool for ultra low leakage levels. MOS capacitors on both n-type and p-type SiC demonstrated comparable gate-oxide leakage. For either type of substrate, the leakage is extremely low, enabling the development of nonvolatile RAMs on SiC.

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