A Novel High Frequency SOI MESFET by Modified Gate Capacitances

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Abstract- A novel SOI MESFET with high frequency performance over conventional structures is presented. The key idea in this work is to control gate capacitances by modifying channel charges. The proposed structure consists of an additional oxide layer in the channel under gate to control the channel charges. We investigate the improvement in device performance with two-dimensional and two-carrier device simulation. The proposed structure improves the gate-source and gate-drain capacitances and the minimum noise figure in comparison with a conventional SOI MESFET (C-SOI). Moreover, it has been decreased the carriers concentrations especially holes around drain. Hence it causes the generation rate decreases by 137% near the source side with a minimum value around the oxide and therefore the break down voltage will increase. The results demonstrate that the proposed structure has better frequency characteristics in comparison with the C-SOI structure.

*Index Terms-*Modified gate capacitances; MESFET; silicon-on-insulator; high frequency.

I. INTRODUCTION

The Metal Semiconductor Field Effect Transistor (MESFET) fabricated on Silicon-On-Insulator (SOI) has been considered as one of the important candidate for excellent RF performance. It has been considered by large number researchers for more than decades [1-6] because this has the significant advantage of being compatible with mainstream CMOS processing and widely used for ULSI/VLSI application.

SOI MESFETs also provide high voltage, low noise, high speed performance, and better frequency comparing with MESFET structures [7].

Recently, significant effort has been reported for improving the characteristics of this technology such as double-recessed structure, field plate structure, source –field plate structure, T-gate and so on [8-12].

In this paper the challenge is to improve cut-off Frequency (f_T), maximum oscillator frequency (f_{max}) and minimum noise figure (F_{min}) of MESFETs. One way for having better frequency parameters is decreasing gate-source and gate-drain capacitance, which will reduce if the channel charges are controlled.

In order to improve the SOI-MESFET structure without increasing the dimensions and to have a high frequency device, a novel SOI-MESFET structure with an oxide region in the channel region is proposed. A proposed structure that consists of the oxide region as an obstacle in the channel can control the charges by modifying the electron and hole concentrations in channel as a result of changing the depletion layer. Therefore, the capacitances will decrease and the RF parameters will improve. We have called the proposed structure as the SOI-MESFET by modified gate capacitances (MGC-SOI). Also, the parasitic bipolar junction transistor (BJT) effect can be controlled by changing

the hole density in the channel and it decreases the impact generation rate therefore the device break down voltage will increase.

II. SCHEMATIC AND SIMULATION

Fig. 1 shows the schematic of the proposed structure. The structure consists of an insulator material (silicon dioxide) is located in the channel to control the channel charges. By changing the length and thickness of insulator in the channel and examining a lot of position and also investigating its effect on power and high frequency parameters, we can find the best location for it at $L = 0.2 \mu\text{m}$ and $t_{\text{ox}} = 0.1 \mu\text{m}$. By changing length of additional oxide and increasing it compared with the optimized value and locating it under gate electrode, the channel capacitance (C), including gate-drain and gate-source capacitance, increased as a result of increasing its area. The values of high frequency considerably depend on the gate-source and gate-drain capacitances, so by increasing C the f_t and f_{max} which are inversely proportional to C are getting worse and F_{min} which are direct proportional to it decreased. By decreasing length from $0.2 \mu\text{m}$ there is a nuance improvement in high frequency parameters but it omitted the effect of improving the V_{BR} , so the best consequent length on both power and frequency parameters achieved in $L = 0.2 \mu\text{m}$. In addition by increasing t_{ox} , the channel capacitance increased and degradation on high frequency parameters occurred, also the power of device decreased as a result of inducing I_{Dsat} . So the increase of t_{ox} has negative effect on parameters. Although by decreasing t_{ox} high frequency improved but the device cannot tolerate high voltage and V_{BR} is lower than the maximum value, so the best result for it achieved in $0.1 \mu\text{m}$. Other structure dimensions are the distance between the oxide layer and device left end $D = 0.5 \mu\text{m}$ and the spacing between oxide and device surface is zero. All the simulation parameters of the proposed structure are given in Table I.

A temperature of 300 K is employed by default in the simulations. All the device

parameters of the MGC-SOI MESFET are equivalent to those of the C-SOI MESFET unless otherwise stated.

The 2-D numerical simulations are done with Atlas from Silvaco [13]. In order to achieve realistic results several models are activated in the simulation, including: Shockley–Read–Hall recombination (SRH model), Auger recombination (Auger model), concentration- and temperature-dependent mobility (Analytic model), parallel electric-field-dependent mobility (Fldmob model), incomplete ionization (incomplete model), band-to-band high electric field tunneling (BBT-STD model), Lombardi mobility (CVT Model), impact ionization (impact Selb model).

It is worth noting that the 2-D simulator is calibrated to experimental data. The output characteristics extracted from experimental measurement have been compared with simulation in Fig. 2. It can be seen from the figure that a good agreement between experimental data [14] and simulation results is achieved.

III. RESULT AND DISCUSSION

A. *Modified Gate Capacitances*

Generally, in the absence of source-drain voltage there is a uniform depletion layer and it is controlled by the gate voltage. Fig. 3 (a) and (b) shows the difference between the depletion layers of C-SOI and MGC-SOI MESFET structures and the effect of oxide region on the channel. In the C-SOI MESFET if the gate bias is fixed and the drain voltage is increased toward positive values, the current starts to flow in the channel and the depletion layer becomes larger near the drain side. As the drain voltage increases more, the depletion width toward the drain end expands. Therefore the carriers concentrations increase in the channel especially between gate and drain end [15]-[16]. The channel then starts to pinch off at drain side and finally the current will be saturated,

but the oxide region causes this process occurs at higher drain voltage in the MGC-SOI MESFET. The oxide has a large band gap and it is a barrier for carriers, so the carriers could not flow inside it and even the carrier density will be changed around it in the channel. Fig. 4 shows the carriers concentrations at the channel surface of proposed structure in presence of oxide region under gate in comparison with C-SOI MESFET.

It transvers different path for two carriers around oxide, electrons have the same concentration as conventional one but hole density after oxide will be less than old one because the presence of oxide eliminate some holes.

By changing carrier concentration, the channel conductance and depletion layer will change. 2-D of current density for the C-SOI and MCC-SOI MESFET structures are shown in Fig. 5 under a bias condition of $V_{GS} = -6$ V and $V_{DS} = 19$ V. As can be seen from the figure as a result of changing depletion layer between the active layer and BOX, the current density and the effective value of the channel thickness change. Therefore the drain voltage in proposed structure will be higher than the C-SOI MESFET.

The understanding of impact ionization and impact generation rate is important for both device degradation and breakdown studied. The number of electron and hole pairs generation by impact ionization is proportional to the maximum electric field (E_{max}) and carrier concentrations. Both the mobile carriers and the strong electric field are required for impact ionization to occur. Indeed, the generation along channel current path will follow the electric field lines and the main impact ionization occurs around the region with maximum electric field at the drain edge of the gate or inside the high field domain along the conduction channel where the electric field is high and the current density is highest [17]-[18]. So the electrons accelerate with high velocity that causes the impact ionization and creates electron-hole pairs.

By fixing gate bias and increasing drain voltage, the potential different between the gate and the drain end of the channel increases, eventually at high drain voltage equal to

breakdown voltage (V_{BR}), the E_{max} occurs and the electric field lines will be closer. The maximum voltage that can be supported by a power device before the onset of significant current flow is limited by breakdown voltage. In the MGC-SOI MESFET the charges and current density in the channel decreases especially at the drain edge of gate, so as shown in Fig. 6 the electric field lines will scatter. Fig. 7 shows the equipotential contours at the break down voltage and $V_{GS} = -5$ V for both the structures. The figure shows effect of the additional oxide in spreading the potential lines towards the drain at the proposed structure. It is worth noting that the lines crowding at the gate edge is weak in the MGC-SOI MESFET structure due to the effect of the locating oxide under gate compared with the C-SOI MESFET structure. So the drain voltage has significant improvement in comparison with the conventional structure. It clearly shows that the increase of breakdown voltage is attributed to scattered electric field crowding at gate corner near drain, therefore the proposed structure can tolerate much higher voltage. As can be seen from Fig. 8, the V_{BR} increased from 13 V to 19 V which is increased by about 46% compared to the C-SOI MESFET. Typical applications for power devices desired to controlled larger power levels and have encouraged the development of power devices with larger breakdown. Also, SOI technology suffers from a low breakdown voltage and it can be solved by changing electric field distribution, so the proposed structure can be an excellent candidate for power design.

Knowledge of electric field distribution along conduction path is essential for the study of impact ionization because higher electric field causes more generation. 2-D and 3-D impact generation rate for both the structures are shown in Fig. 9 at $V_{GS} = -6$ V and $V_{DS} = 19$ V. The figure shows that the generation rate is decreased by 137% near the source side with a minimum value around the oxide under gate near drain side as a result of reducing carriers and scattering electric field lines. Also, the parasitic bipolar transistor amplifies the hole current that is generated by the impact ionization and degrades the performance

of the SOI MESFET. By decreasing the hole density and impact generation in the channel, the effect of parasitic bipolar transistor decreases in the MGC-SOI MESFET. So the proposed structure can be used in high power, high temperature and microwave frequency applications [19]-[20].

B. High frequency characteristics

The cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) are two main parameters in high frequency characteristics of devices. The expressions for the f_T and f_{max} are as following [21]-[22] :

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD} + C_{par})} \quad (1)$$

$$f_{max} = \frac{f_T}{2} \sqrt{\frac{R_{DS}}{R_G}} \quad (2)$$

where the element $C_{GS} + C_{GD}$ are the total gate-channel capacitance and C_{par} is the parasitic input capacitance. R_{DS} and R_G are the output resistances under the gate and gate resistances, respectively. Also g_m is transconductance. The values of the f_{max} and f_T considerably depend on the gate-source and gate-drain capacitances.

Fig. 10 shows the gate-source and gate-drain capacitances versus the frequency for the proposed structure and conventional one at $V_{GS} = 0$ V and $V_{DS} = 8$ V. As can be seen from the figure, the gate-source and gate-drain capacitances of the MGC-SOI MESFET are reduced by 33% and 66%, respectively in comparison with the C-SOI MESFET due to reduction of the channel charges. So the frequency parameters in the MGC-SOI MESFET improve as reported on Table II under $V_{GS} = 0.5$ V and $V_{DS} = 8$ V.

It is important to design a device with low noise parameters. The MESFET is a low-noise device, due to only majority carriers participate in the operations, and the carriers transport through the channel in the bulk and are free of surface or interface scattering. In

practical devices, extrinsic and parasitic resistances are unavoidable, which are mainly responsible for the noise behavior.

One method of defining the noise performance of an amplifier is the noise figure (F).

This can be defined as the ratio of equivalent noise power developed at the input to that generated by noise in the source resistance (R_s), also it depends on the circuitry external to the device. There is an important parameter called the minimum noise figure which is obtained with both the source impedance and load impedance being optimized for noise performance. The $F_{\min}$ for a practical device is obtained by the following equation [21]:

$$F_{\min} = 1 + 2\pi C_1 f C_{GS} \sqrt{\frac{R_G + R_s}{g_m}} \quad (3)$$

where C_1 is a constant of value 2.5 s/F and R_s and R_G are the source and gate resistances which g_m and R_G is related to width of channel and R_s is inversely proportional to it.

As mentioned previously, the C_{GS} of the MGC-SOI MESFET, which is an important parameter in the noise analysis, is lower than that of the C-SOI MESFET that leads to the reduction of noise value at the proposed structure. Fig. 11 illustrates the $F_{\min}$ versus frequency and it is clear that the $F_{\min}$ of the MGC-SOI MESFET is lower than that of the C-SOI MESFET. So it can be used in high power and high frequency applications.

V. CONCLUSION

In this article frequency parameters and noise have been analyzed at a novel MESFET structure. In the proposed structure an additional oxide in channel under gate and near drain modified the channel charge and depletion region and decreases the gate capacitances. The decreasing of C_{GS} , C_{GD} has a positive impact on RF characteristics, including f_T , f_{max} , and F_{min} . In addition, it has low generation rate comparing with a conventional SOI MESFET. Therefore, the novel structure has better characteristics compared with conventional structure and it can be used in high power, high speed and microwave frequency applications.

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Table I: Typical device structure parameters for MGC-SOI MESFET

Device Parameters	Symbol	Value
Gate Length	L_G	0.5 μm
Gate-Source spacing Length	L_{GS}	0.5 μm
Gate-Drain spacing Length	L_{GD}	0.5 μm
Source Length	L_S	0.3 μm
Drain Length	L_D	0.3 μm
Oxide Length	L	0.2 μm
Oxide thickness	t	0.1 μm
Distance between the oxide region & device left end	D	1.2 μm
Channel thickness	t_C	0.2 μm
Buried oxide thickness	t_{BOX}	0.4 μm
Substrate thickness	t_s	0.1 μm
Channel doping concentration	N_D	$1.5 \times 10^{17} \text{ cm}^{-3}$
Source/Drain doping concentration	N_D	10^{20} cm^{-3}
Substrate doping concentration	N_A	10^{13} cm^{-3}

Table II: Comparison of frequency parameters between the MGC-SOI and C-SOI

MESFET structures

SOI MESFET Structure	$f_T(\text{GHz})$	$f_{\max}(\text{GHz})$
C-SOI MESFET	35	40
MGC-SOI MESFET	90	94

Figure Captions

- Figure 1 Schematic of MGC-SOI MESFET structure.
- Figure 2 The output characteristic of simulated MGC-SOI MESFET has been compared with experimental results in Ref [14].
- Figure 3 Depletion layer for (a) C-SOI MESFET (b) MGC-SOI MESFET under a bias condition of $V_{GS} = -4$ V and $V_{DS} = 0$ V.
- Figure 4 Comparison concentration of hole and electron along channel for both the structures at $V_{GS} = -5$ V, $V_{DS} = 13$ V conditions.
- Figure 5 2-D current density for (a) C-SOI MESFET (b) MGC-SOI MESFET under a bias condition of $V_{GS} = -6$ V and $V_{DS} = 19$ V.
- Figure 6 Electric field lines of the device from left to right of the device.
- Figure 7 Simulated equipotential contours at the breakdown voltage for (a) C-SOI MESFET (b) MGC-SOI MESFET.
- Figure 8 Three-terminal Breakdown characteristics.
- Figure 9 2-D and 3-D impact generation rate for both the structures in $V_{GS} = -6$ V and $V_{DS} = 19$ V.
- Figure 10 Gate-Source Capacitance (C_{GS}) and Gate-Drain Capacitance (C_{GD}) versus frequency for the proposed structure and conventional one.
- Figure 11 Minimum noise figure (F_{min}) as a function of frequency.

Fig. 1.

Fig. 2.

(a)

(b)

Fig. 3.

Fig. 4.

Fig. 5.

(a)

(b)

Fig. 6.

(a)

(b)

Fig. 7.

Fig. 8.

(a)

(b)

Fig. 9.

Fig. 10.

Fig. 11.

Highlights

A SOI MESFET with high frequency performance is presented.

The key idea is to control gate capacitances by modifying channel charges.

The structure improves the G-S and G-D capacitances and the $F_{\min}$ and decreases them.

It causes the generation rate decreases near the source and drain side in channel.

The structure has superior performances in comparison with conventional structures.

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