Investigation of Electron-Hole Generation in MOS Capacitors on 4H SiC

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Abstract—This paper investigates electron-hole generation in n-type MOS capacitors on 4H-SiC with the gate oxide directly grown in either 100% NO or 10% N₂O. High-temperature capacitance-transient measurements were used to determine and compare the contributions of carrier generation in the bulk and at the SiO₂-SiC interface. The effective generation rate in the bulk is similar in the MOS capacitors with either type of gate oxide, whereas the effective surface-generation rate is much lower in the case of oxides grown in 100% NO. Moreover, the effective surface-generation rate in these oxides is reduced to the level that is comparable to the effective bulk-generation rate. This result demonstrates the high quality of MOS capacitors with the gate oxide directly grown in 100% NO.

Index Terms—Bulk carrier generation, charge-retention time, interface-trap density, MOS capacitor, surface carrier generation.

I. INTRODUCTION

IN SILICON carbide, the carrier-generation rate is extremely low at room temperature. This is because silicon carbide is a wide energy gap material ($E_g = 3.26$ eV in 4H-SiC [1]) with very low intrinsic-carrier concentration ($n_i = 10^{-7}$ cm⁻³ in 4H-SiC [1]). Based on the Shockley-Read-Hall (SRH) theory [2], [3], the generation rate is proportional to n_i , so the generation rate in SiC should be many orders of magnitude lower than in Si [1], [4]. With this low generation rate, it should be possible to minimize the leakage current of reverse-biased P-N junctions to the levels that enable unique applications. One of these applications relates to the development of nonvolatile random-access memories (NVRAMs). Characterizing an NVRAM cell, based on an N-P-N structure in 6H SiC, Wang *et al.* [5] concluded that surface generation at the junction terminations increased the carrier-generation rate well above the value that would be expected in the bulk of a high-quality SiC substrate. Recently, the passivation of SiC surfaces has been considerably improved by using nitrided thermal oxides [6], [7]. Using nitrided gate oxides, extremely long charge-retention times have been experimentally demonstrated for MOS capacitors on 4H SiC [8], [9] and 6H SiC [10].

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In this paper, we use high-temperature capacitance-transient measurements and Zerbst plots to determine the effective surface-generation and bulk-generation rates in SiC passivated by nitrided oxides. The Zerbst plot is widely used for characterization of MOS capacitors on silicon, utilizing straightforward capacitance-transient measurements at room temperature. In the case of SiC, the generation rates are so low that the capacitance-transient measurements have to be performed at high temperatures. To estimate the generation rates at room temperature, it is necessary to use an extrapolation technique. This issue and a suggested solution are considered in Section II of this paper. Section III provides the experimental details, whereas Section IV presents and analyzes the results for MOS capacitors with gate oxides obtained by two different techniques: direct growth in 100% NO and direct growth in 10% N₂O. These are the best NO-based and N₂O-based nitridation techniques, according to surface-roughness measurements [7], [11], reliability investigations [6], and the values of interface-trap densities [7], [11]. The effective surface-generation rates are compared to the typical value in Si and to the simultaneously-determined bulk-generation rates, in order to draw the conclusions about the interface quality obtained by these two nitridation techniques. Also, the charge-retention times for depleted MOS capacitors are determined to demonstrate that nonvolatile RAMs can be developed in SiC.

II. ESTIMATING EFFECTIVE BULK-GENERATION AND SURFACE-GENERATION RATES IN SiC

In thermal equilibrium, the carrier generation rate is equal to the carrier recombination rate. When a MOS capacitor is pulsed from accumulation into deep depletion, the recombination rate is reduced to insignificant levels due to the depletion (or absence) of carriers that would recombine each other. As the generation mechanisms continue to act, the generated minority carriers are being collected at the semiconductor surface. This is the process that will ultimately create the inversion layer at the semiconductor surface with the carrier density that corresponds to the equilibrium condition. The rate of increase of the carrier density in the inversion layer, dN_I/dt , can be defined as the effective generation rate. Although this rate is in the units of cm⁻²s⁻¹, it involves the contributions of the bulk generation (in the bulk of the depletion layer) as well as the surface generation. In fact, four different generation components can be identified [12]:

- 1) generation in the bulk of the depletion layer;
- 2) surface generation in depletion layer under the gate;
- 3) lateral surface generation (outside the gate area);

- 4) quasineutral bulk generation that is related to back-surface generation.

The usual model for the effective generation rate can be written as [12]

$$\frac{dN_I}{dt} = \frac{n_i(W - W_{inv})}{\tau_g} + n_i s_g + \frac{n_i s_g A_S}{A_G} + \frac{n_i^2 D_p}{N_D L'_p}. \quad (1)$$

The first term in (1) models the generation in the bulk of the depletion layer, where n_i is the intrinsic-carrier concentration, W_{inv} is the depletion-layer width at thermal equilibrium when the inversion layer is fully formed, W is the actual (variable) depletion-layer width, and τ_g is a parameter. The parameter τ_g is usually called *generation lifetime* [12], but this name can wrongly suggest that the time needed to create the inversion layer (due to the bulk generation) is in the same order of magnitude as τ_g . In SiC, τ_g can be shorter than in Si (shorter than a microsecond), yet the time needed to create the inversion layer may still be longer than a billion of years. According to the SHR theory, the bulk-generation rate (in the units of $\text{cm}^{-3}\text{s}^{-1}$) can be expressed as n_i/τ_0 , where τ_0 is the sum of the electron and hole minority-carrier lifetimes [13]. The physical meaning of the minority-carrier lifetime is well established: it is the average time an excess minority carrier will live in a sea of majority carriers [13]. Therefore, it is not surprising that a material with as wide energy gap as SiC can have a shorter minority-carrier lifetime than Si. The bulk-generation term n_i/τ_0 is modified in (1) by multiplying it by $W - W_{inv}$, so that

- 1) the rate is expressed per unit area ($\text{cm}^{-2}\text{s}^{-1}$) rather than per unit volume;
- 2) the rate decays to zero as the thermal equilibrium is approached.

Because of this change, the parameter τ_g is not equivalent to τ_0 , but nonetheless, its value remains close to the value of the minority-carrier lifetimes.

The second term in (1) models the surface generation in the depletion layer under the gate, where s_g is the related parameter. According to the SHR theory, the surface generation rate (in the units of $\text{cm}^{-2}\text{s}^{-1}$) is equal to $s_0 n_i$, where s_0 is the surface recombination velocity (because we deal with effective generation in the depletion layer, s_0 is also called the *surface generation velocity*) [13]. The parameter s_g is not identical to s_0 because it has to ensure that the effective surface generation approaches zero as the thermal equilibrium is approached. Nonetheless, the value of s_g is close to the surface recombination velocity, s_0 , in the area of interest (away from the thermal equilibrium).

The third term in (1) models the surface generation outside the gate area (lateral surface generation), where A_G is the area under the gate and A_S is the area of the depletion layer surrounding the gate at the surface of the semiconductor. Using large-area capacitors, the factor A_S/A_G can be made small enough so that this term can be neglected. This approach is different from the approach by Pan *et al.* [14] who used capacitors with different perimeters to determine the surface-generation rate at the gate perimeters.

The fourth term in (1) models the quasineutral bulk generation, related to the back-surface generation, where D_p is the diffusion coefficient of minority carriers, L'_p is either the diffu-

sion length or the wafer thickness (whichever is smaller), and N_D is the doping level. Given that the intrinsic-carrier concentration is very small in SiC, n_i^2 is so small that this term can also be neglected.

After these considerations, (1) can be simplified to

$$\frac{dN_I}{dt} = \frac{n_i(W - W_{inv})}{\tau_0} + n_i s_0 \quad (2)$$

where the first term is the effective bulk-generation rate (G_B) and the second term is the effective surface-generation rate (G_S), with the minority-carrier lifetime (τ_0) and the surface-recombination velocity (s_0) as the related parameters.

Given that the depletion-layer width changes as the minority carriers are generated and take place in the inversion layer, the capacitance of the MOS structure changes in time. The capacitance change can be measured and presented as the well-known Zerst plot, $-d(C_{ox}/C)^2/dt$ versus $C_{inv}/C - 1$, where C is the measured capacitance, C_{ox} is the gate-oxide capacitance, and C_{inv} is the capacitance at inversion level [12], [15]. The Zerst plot has a linear region in the middle, with a curved portion near the origin when the device approaches equilibrium and a curved portion at the other end due to field-enhanced emission from interface and/or bulk traps [16], [17]. The first term in (2) depends on the depletion layer width, so its parameter (τ_0) can be extracted from the slope of the linear part of the Zerst plot. The second term in (2) is independent of W , so its parameter (s_0) can be extracted from the intercept of the extrapolated straight line on the vertical axis.

The use of the Zerst plot is well documented for the case of silicon. A problem in silicon carbide is that the generation rates are so low that no capacitance change can be measured at room temperature. This problem can be solved by measurements at high temperatures, but the parameters τ_0 and s_0 in (2) that can be obtained from the Zerst plots, are clearly high-temperature values. Therefore, it is necessary to establish the temperature dependencies of τ_0 and s_0 , in order to enable extrapolations to room temperature.

Given that the parameter of the bulk generation process is close to the minority-carrier lifetime in (2), its temperature dependence can be established from the following equation [13], [18]

$$\tau_0 = \frac{1}{\sigma v_{th} N_T} \quad (3)$$

where σ is the capture cross section for the minority carriers, v_{th} is the thermal velocity, and N_T is the midgap concentration of recombination-generation centers. The capture cross section is temperature dependent and it is best fitted with the Arrhenius-type equation [19]

$$\sigma = A \exp\left(\frac{-E_\sigma}{kT}\right) \quad (4)$$

where kT is the thermal energy, A is a constant, and E_σ is the capture cross-section activation energy. The thermal velocity, v_{th} , is also temperature dependent

$$v_{th} = \sqrt{\frac{3kT}{m^*}} \quad (5)$$

where m^* is the carrier effective mass. With these, τ_0 can be expressed as

$$\tau_0 = \frac{1}{A \exp\left(\frac{-E_\sigma}{kT}\right) \sqrt{\frac{3kT}{m^*}} N_T}. \quad (6)$$

Based on this result, the high-temperature values for τ_0 should be plotted as $-\ln(\tau_0 T^{1/2})$ versus $1/kT$ to enable the extraction of the activation energy and the extrapolation of τ_0 to room temperature.

Analogously, the equation for the surface-recombination velocity can be used to determine the temperature dependence of s_0 [13]

$$s_0 = \frac{\pi}{2} \sqrt{\sigma v_{th}} kT D_{it}(E_i) \quad (7)$$

where $D_{it}(E_i)$ is the interface-trap density at the midgap. Substituting (4) and (5) into (7), the temperature dependence of s_0 is obtained as

$$s_0 = \frac{\pi}{2} \sqrt{A} \sqrt{\exp\left(\frac{-E_\sigma}{kT}\right)} \left(\frac{3k}{m^*}\right)^{1/4} T^{1/4} kT D_{it}(E_i). \quad (8)$$

Therefore, the high-temperature values for s_0 can be plotted as $\ln(s_0^2/T^{2.5})$ versus $1/kT$ to enable the extraction of the activation energy and the extrapolation of s_0 to room temperature.

III. EXPERIMENTAL DETAILS

MOS capacitors were fabricated on Si-faced, n-type 4H-SiC wafers with 3- μm thick epilayer doped with nitrogen (doping concentration of $1.0\text{--}1.8 \times 10^{16} \text{ cm}^{-3}$). The 8° off (0001) oriented wafers were purchased from CREE Research Inc. They were first cleaned in a mixture of H_2SO_4 and H_2O_2 , followed by an RCA clean. Immediately prior to oxidation, the wafers were dipped in 1% HF for 1 min. Two types of nitrided gate oxides were separately grown in a standard horizontal furnace by two different processes. The first type of nitrided gate oxide was directly grown in 10% nitrous oxide (N_2O), diluted in 90% N_2 at 1300°C for 4.5 h (labeled as “10% N_2O ”). The second type of nitrided gate oxide was directly grown in 100% nitric oxide (NO) for 1 h at 1175°C , followed by 2 h 15 min of dry oxidation, and final 2 h of direct 100% NO grown (labeled as “100% NO”) [7]. After the oxide growth, the samples were cooled down to 800°C in high-purity N_2 at approximately $5^\circ\text{C}/\text{min}$. Subsequently, aluminum was thermally evaporated to form the gate electrodes. MOS capacitors were then defined by photolithography. The area of the capacitor gates (A_G) was 200 times larger than the estimated surface area of the depletion layer at the perimeter of the gate (A_S). This enabled us to neglect the third term in (1), as discussed in Section II. Finally, a large area of aluminum back contact was thermally evaporated on the n^+ substrate.

The MOS capacitors were characterized by high-frequency (100 kHz) capacitance-voltage (HF C - V) measurements, with sweep rate of 0.1 V/s and sweep range from 5 V to -5 V, using a computer-controlled HP4284A LCR meter. The gate-oxide thicknesses, determined from the accumulation capacitances, were 27 nm and 24 nm for the 10% N_2O and the 100% NO

Fig. 1. Comparison of flatband-voltage shifts (ΔV_{FB}) measured at different temperatures for oxides grown in 10% N_2O and 100% NO.

oxides, respectively. The HF C - V curves were measured at different temperatures (ranging from 300 K to 630 K) and the flatband-voltage shifts from the ideal curve (ΔV_{FB}) were determined for both types of oxides (Fig. 1). The ideal C - V curve was obtained by the method described in [12]. There were not significant dependencies of the flatband-voltage shifts on temperature for either type of oxide, indicating good stability of these oxides at high temperatures.

In order to obtain the capacitance-transient (C - t) measurements, the MOS capacitors were heated at different high temperatures ranging from 523 K to 628 K, so that the generation process is accelerated. At these temperatures, the capacitor is initially biased at accumulation and then instantly stepped to a reverse-bias voltage corresponding to deep depletion. A computer-controlled HP4284A LCR meter recorded the capacitance changes from deep-depletion level (C_{dd}) to inversion (C_{inv}) level with time, at a constant gate voltage ($V_G = -5$ V, corresponding to the surface potential $\varphi_s = -4.20$ eV). The C_{dd} and C_{inv} were theoretically calculated from the HF C - V curves [12] and matched to the measured deep-depletion and accumulation levels [8], [9]. All the measurements were performed in dark environment to eliminate the possible contribution from photon generation. Prior to transforming high-temperature C - t data to Zerst plots, the raw data were first smoothed by Kernel Smoothing Method [20]. After that, the minority-carrier lifetime and the surface-generation velocity were extracted.

IV. RESULTS AND DISCUSSION

A. Minority-Carrier Lifetime and Surface-Recombination Velocity

The results of the high-temperature C - t measurements are presented in Fig. 2 for both types of nitrided oxides. Typical Zerst plots, obtained from these data, are shown in Fig. 3. The curved parts near the origins follow the usual pattern observed in Si when the capacitance approaches its equilibrium level (C_{inv}). The far-end parts of the plots, that are due to the field-enhanced emission from interface traps [16], [17], show strong increases that are similar to the behavior observed by Neudeck *et al.* for dry oxides on 6H SiC [21]. The increases are

Fig. 2. High temperature C - t measurements for (a) 10%- N_2O grown oxide and (b) 100%-NO grown oxide.

significant in comparison to a typical plot in Si samples [15], indicating that the interface-trap density is much higher in SiC. The middle parts of the Zerst plots, needed for the extraction of τ_0 and s_0 , are relatively linear. The extracted values for τ_0 and s_0 are presented in Figs. 4 and 5, respectively. The plots in Figs. 4 and 5 are prepared according to the temperature dependencies of (6) and (8), to enable extrapolations to room temperature. The coefficient of determination, r^2 , [22] is provided for each plot to indicate how well the regression model describes the data.

Table I presents the extracted room-temperature values for τ_0 and the calculated room-temperature values for the effective bulk-generation rate, G_B , by using $n_i = 1.6 \times 10^{-7} \text{ cm}^{-3}$ [1] and $W - W_{inv} = 9.4 \times 10^{-6} \text{ cm}$. The values for τ_0 and G_B are comparable for both types of oxides, which is an expected result given that τ_0 relates to the quality of the SiC substrate and is not a parameter that should depend on the gate oxide processing.

The estimated room-temperature values for s_0 are also presented in Table I. The value for the 100%-NO grown oxide ($\sim 10^0 \text{ cm/s}$) is approximately three orders of magnitude lower than for the 10%- N_2O grown oxide ($\sim 10^3 \text{ cm/s}$). According to (7), s_0 is directly related to the interface-trap density at the midgap, $D_{it}(E_i)$. The HF C - V measurements conducted at room temperature (Fig. 6) show differences in the slopes of the

Fig. 3. Zerst plots constructed using C - t measurement acquired at 628.15 K (355 °C) for oxides grown in (a) 10% N_2O and (b) 100% NO.

C - V curves that can be related to the interface-trap density. It can be seen that the C - V curves of the 100%-NO grown oxide are steeper, indicating a lower $D_{it}(E_i)$, in agreement with the lower s_0 value. Quantitative measures of the densities of the interface traps, located between 0.22 eV and 0.60 eV below the bottom of the conduction band, were obtained by the conductance technique at 523 K and the results are shown in Fig. 7. The lower interface-trap density in this energy range, observed for the case of 100%-NO oxides, also indicates a lower density of the interface traps at the midgap (the D_{it} value at midgap cannot be measured using the conductance technique, so we assume that the D_{it} distribution at midgap follows the same trend shown in Fig. 7). It should be noted that the value of $s_0 \sim 10^0 \text{ cm/s}$, obtained with the oxide grown in 100% NO, is higher than the typical surface-recombination velocity in MOS capacitors on silicon (usually about 0.2 cm/s [12]). This is due to the fact that the interface-trap density at nitrided SiC-SiO₂ interfaces is still higher than at a high-quality Si-SiO₂ interface. The higher interface-trap density in MOS capacitors on SiC also relates to the observed steep increase at the end part of the Zerst plot that is caused by the field-enhanced emission from the interface traps. Nonetheless, when the s_0 values of the nitrided oxides are used to calculate the effective surface-generation rates, G_S , the following results are obtained: $\sim 10^{-7} \text{ s}^{-1} \text{ cm}^{-2}$ for the

Fig. 4. Minority-carrier lifetime, τ_0 , as a function of temperature for oxides grown in (a) 10% N_2O and (b) 100% NO .

100%-NO grown oxide and $\sim 10^{-4} \text{ s}^{-1} \text{ cm}^{-2}$ for the 10%- N_2O grown oxide (Table I). For the case of the oxide grown in 100% NO , the effective surface-generation rate is comparable to the effective bulk-generation rate. This is a very important result, showing that SiC-SiO₂ interface can be passivated so to prevent excessive charge leakage due to surface generation or recombination.

B. Charge-Retention Time in MOS Capacitors Used as Memory Elements

MOS capacitors can be used as charge-storage elements in memory devices. The deep-depletion capacitance level (C_{dd}) can be defined as the logic 1 level, whereas the inversion capacitance level (C_{inv}) can be defined as the logic 0 level. Given that C_{inv} is the capacitance in thermal equilibrium, the charge-retention time of a MOS capacitor used as a memory element is determined by how long it takes for the capacitance to change from the deep depletion to the inversion state. The charge-retention characteristics of the fabricated MOS capacitor were investigated using the thermally accelerated capacitance-transient (C - t) measurements described in Section III. The exponential increase of capacitance (C) with time (t) at a particular temperature is approximated by [8]–[10]

$$C = C_{inv} - \Delta C [\exp(-t/\tau)] \quad (9)$$

Fig. 5. Surface-recombination velocity, s_0 , as a function of temperature for oxides grown in (a) 10% N_2O and (b) 100% NO .

TABLE I
ESTIMATED ROOM TEMPERATURE VALUES FOR τ_0 , s_0 , G_B , G_s , AND CHARGE-RETENTION TIME

Parameter	Unit	10% N_2O	100% NO
τ_0	s	10^{-6}	10^{-6}
s_0	cm/s	10^3	10^0
Effective bulk-generation rate, G_B	$\text{s}^{-1} \text{ cm}^{-2}$	10^{-7}	10^{-7}
Effective surface-generation rate, G_s	$\text{s}^{-1} \text{ cm}^{-2}$	10^{-4}	10^{-7}
Room temperature retention time measured at $\phi_s = -4.20 \text{ eV}$	year	10^9	10^{10}

where $\Delta C = C_{inv} - C_{dd}$ and τ is the charge-retention time [8]–[10]. As mentioned earlier, the thermal generation process in SiC is extremely low, so high temperature measurements are needed. In order to extract the charge-retention time at room temperature, The Arrhenius-type temperature dependence was assumed [8]–[10]

$$\tau = Z \exp\left(-\frac{E_A}{kT}\right) \quad (10)$$

where Z is a constant and E_A is the corresponding activation energy.

Fig. 6. Typical high frequency C - V measurements.

Fig. 7. Comparison of interface-trap density (D_{it}) measured at 523 K by conductance technique for oxides grown in 10% N_2O and 100% NO .

Fig. 8 presents the Arrhenius plots for the charge-retention times, measured at a constant applied gate voltage, for the two types of nitrided oxides. There is a significant difference between the extracted charge-retention times (at room temperature) for the two nitrided oxides, with the 10%- N_2O grown oxide having approximately an order of magnitude shorter charge-retention time ($\sim 10^9$ years) than the 100%- NO grown oxide ($\sim 10^{10}$ years) (Table I). This is in agreement with the values for the surface-recombination velocities and the interface-trap densities, presented in Section IV-A. Importantly, the charge-retention times in either oxide are long enough to enable the use of these MOS capacitors on SiC as memory elements.

V. CONCLUSION

We have investigated the electron-hole generation in an n-type MOS capacitor with oxides either grown in 100% NO or 10% N_2O on 4H SiC by high-temperature capacitance-transient measurements. The contributions of carrier generation in the bulk and at the SiO_2 -SiC interface are evaluated and compared. While the effective bulk-generation rates are approximately equal for both types of nitrided oxides, the effective surface-generation rates show very strong dependencies on the

Fig. 8. Arrhenius plots for the extrapolation of the charge-retention times to room temperature. The surface potential for all measurements is -4.20 eV. The coefficient of determination, r^2 , of each plot is shown.

type of oxide and the associated interface-trap densities. In the case of the oxides grown in 100% NO , the effective surface-generation rate is reduced to the level that is comparable to the effective bulk-generation rate. Extremely long charge-retention times are obtained with either oxidation process, demonstrating that nonvolatile RAMs can be developed in SiC.

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