Properties of Nitrided Oxides on SiC

S. Dimitrijević, H.B. Harrison, P. Tanner, K.Y. Cheong, and J. Han

INTRODUCTION

If there is a singular property of silicon that has contributed to its success as a semiconductor material, it is the native oxide, SiO_2 . This oxide can be thermally grown to form an effective insulating layer as part of the gate in a MOSFET structure. Silicon Carbide also has the ability to grow a similar oxide, and when combined with the bulk properties of wide bandgap high thermal conductivity and extremely low intrinsic free carrier concentration, will lead to an enormous number of applications. This means that as far as the gate oxide is concerned SiC can be processed in much the same way as Si, the exception being that the processing temperatures are generally higher.

A major obstacle to the formation of a high quality oxide on SiC is the role that carbon plays during the oxide growth. Thermal oxidation in a wet or dry atmosphere results in residual carbon in the oxide layer and carbon clusters at the oxide-SiC interface. It has been found that oxidation or post oxidation annealing in a nitrogen-containing atmosphere has two beneficial effects – enhanced removal of carbon, and passivation of silicon dangling bonds [1]. The most effective gases in achieving this effect have been nitric oxide (NO) and nitrous oxide (N_2O).

This chapter reviews the recent results on nitrided oxides on SiC. Initially, the various growth techniques are reviewed and compared to show the steps that gave the best result. Then the properties deduced from physical characterization of nitrided oxides are discussed to reveal the way nitrogen is bonded in the oxide and at the interface. The role that nitrogen plays in the removal of carbon during oxidation is also examined. This is followed by a discussion of interface and near-interface traps measured by a range of electrical techniques. Finally, benefits of nitridation of gate oxides used to form MOSFET's and charge storage devices are discussed.

GROWTH OF NITRIDED OXIDES

The quality of oxides on SiC, and the beneficial effects on the near surface bulk properties, has been steadily improving as more is discovered about the growth kinetics and interface reactions. Early attempts to nitride the oxide by annealing in N_2O were not very successful, resulting in a deterioration of electrical properties [2],[3]. However more recently, the use of NO and different N_2O processes has produced a significant improvement in both the bulk oxide and oxide-SiC inter-

face quality. Table 1 summarizes the historical evolution of the nitridation process.

Process	Effect on oxide quality	References
Annealing in N_2O	deterioration of electrical properties.	[2],[3]
Annealing in NO (thin oxides, no epi layer)	improvements in electrical properties.	[4], [5]
Direct growth in N_2O	improvement in electrical properties.	[6], [7]
Direct growth in NO	shown as the best process in terms of interfacial properties and oxide reliability.	6H-SiC[9] 4H-SiC[10]
Diluted N_2O	Good oxide reliability; comparable to NO-grown	[1]
High-temperature growth in N_2O ($>1200^\circ C$)	Reduce interface states and increase MOSFET electron mobility.	[8]
Jet vapour deposition (JVD)	Reduced Dit in upper half of energy gap. Reduced sub-oxides and dangling bonds at interface.	[11]
NO/ O_2 /NO sandwich process	MOSFETs with low field mobility = $48\text{cm}^2/\text{Vs}$; Dit = $3 \times 10^{11}\text{cm}^{-2}\text{eV}^{-1}$; oxide breakdown = 9MV/cm .	[13], [14]
Nitrogen radical treatment	Improved field effect mobility in 4H- and 6H-SiC	[12]

Table 1. Historical comparison of various nitridation techniques and their effects on electrical properties.

It was found by a number of research groups that annealing of dry oxides in NO reduces interface traps and improves oxide reliability, while similar annealing in N_2O has a deleterious effect. These early results were performed on thin oxides on bulk SiC without epi-layers [4], [5]. On the other hand, direct growth of the oxide in N_2O has proven beneficial as N_2O breaks down into O_2 , N_2 and NO at the oxidation temperature [6], [7], particularly above $1200^\circ C$ [8]. It has been proposed that in an N_2O ambient, there exists two competing processes: oxidation via O_2 producing carbon buildup and nitridation via NO assisting in carbon removal [1]. The optimum oxidation process appears to occur when the kinetics for carbon removal are just sufficient to keep pace with carbon generation which is linked to the oxidation rate. The best results on interface quality and oxide reliability to date have been from direct oxide growth in NO, both for 6H-SiC [9] and 4H-SiC [10]. Due to the very slow growth rate of the oxide in NO (5 hours at $1175^\circ C$ to grow 16nm), there is sufficient time for the nitrogen to remove excess carbon. This slow growth rate and the toxic nature of 100% NO means the process may not be desirable for industrial use. If NO presence during the oxide growth is de-

sirable, then the question is what minimum level is required for efficient nitridation of the interface and carbon removal. Fortunately, dilution of N_2O in nitrogen to achieve the desired amount of NO has been found to produce good results [1]. Fig. 1 compares the linear growth rate constants for oxide growth in 100% NO and N_2O , with the calculated activation energies of 3.0 eV and 2.8 eV respectively.

As well as conventional thermal oxide growth, a number of other methods have provided workable gate oxides on SiC. Jet vapor deposition (JVD) of oxide-nitride-oxide stacks on an ultra-thin nitride produced improved interface properties and evidence of nitrogen at the interface and possible N-C bonding [11]. Interface state densities near the conduction band were reduced to below $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. In another case, dry oxides were exposed to nitrogen radicals generated by remote plasma and the resulting MOSFETs showed improved channel mobility [12]. To overcome the low growth rate of oxide in NO, the so-called 'sandwich process' was used, consisting of an initial growth period in NO followed by the main growth in dry oxygen, and then completed with an NO anneal. This process produced a MOSFET low field electron mobility of $48 \text{ cm}^2/\text{Vs}$, low interface state densities, and a dielectric breakdown field strength of 9 MV/cm [13], [14].

Fig. 1 Arrhenius plots for linear oxide growth in NO and N₂O and the extracted activation energies [1].

PHYSICAL CHARACTERIZATION

With the vastly different growth kinetics of thermal oxides on SiC compared to Si, it is important to determine the amount of nitrogen and its distribution relative to the interface. In the Si case, Si≡N bonds passivate the dangling Si bonds. Fig 2 compares the SIMS profiles of nitrogen and oxygen through the oxide-semiconductor interface of both Si and SiC samples nitrided in NO. The nitrogen distribution relative to the interface is exactly the same in both cases, but the percentage of N in SiC is greatly reduced [15].

Fig. 2 Normalized SIMS profiles of oxygen (top) and nitrogen (bottom) in nitrided oxides on Si (symbols) and SiC (lines). The nitrogen peak shape and position are the same relative to the oxygen profiles [15].

The question then is So how the nitrogen is bonded at the oxide-SiC interface. Fig 3 compares XPS spectra for Si 2p at the interface of argon and NO annealed dry oxides on 4H-SiC samples [16]. The argon annealed sample has a broader and more complex peak than the NO annealed sample. A similar difference was also seen in the oxygen and carbon peaks. This indicates that NO annealing of the oxide creates a cleaner interface with less sub-oxides compared to annealing in an

inert gas such as argon. There is also evidence that Si $\equiv$ N bonding occurs at the interface in NO annealed oxides on SiC, as demonstrated in Fig 4 which shows the N 1s peak at 397.8eV. This is very close to the energy of the Si $\equiv$ N bonding in silicon nitride.

(a)

(b)

Fig. 3 (a) Si 2*p* XPS spectrum at the NO annealed SiO₂/SiC interface. (b) Si 2*p* XPS spectrum at the Ar annealed SiO₂/SiC interface [16].

Fig. 4. N 1*s* XPS spectrum at the interface of NO annealed sample, N-1 is the spectrum for Si≡N [16].

Another physical effect of nitridation is smoothing of the interface, as shown in the atomic force microscope images of Fig. 5. Removal of the dry oxide and nitrided oxide layers revealed a significantly smoother SiC surface in the nitrided case, with a mean square roughness of 0.1322nm compared to 0.5778nm for the dry oxide [14]. This is thought to be due to the more efficient carbon removal during oxide growth in the nitrided case and hence reduced formation of carbon clusters at the interface.

Fig. 5. AFM topography for (a) dry oxide and (b) nitrided oxide. The root-mean-square roughness are 0.5778 nm and 0.1322 nm, respectively.

INTERFACE AND NEAR-INTERFACE DEFECTS

Having discussed the physical effects of nitridation on the oxide-SiC interface, we now look at the benefits to the electrical properties of the oxide and its interface with SiC. A major hurdle to be overcome in the development of a viable SiC MOSFET is the reduced channel mobility caused by high densities of interface and near-interface traps. As the different polytypes have differing energy gaps, the energy level of traps with respect to the energy gap means they are electrically active in some polytypes but not in others [17]. For instance, traps with energies just below the conduction band of 4H-SiC are not active in the case of 3C-SiC as they are placed above the conduction band edge, as shown in Fig. 6 [18].

Fig. 6. Interface-trap density, D_{it} as a function of energy for identically processed 3C (001)–4H (11-20)–SiC MOS capacitors [20].

Various studies have linked certain physical defects to the energy location of traps in the energy gap. Traps in the lower half of the energy gap are thought to be related to carbon compounds [19]. Near to the conduction band of 4H-SiC, high densities of predominantly near-interface traps are thought to be responsible for the poor inversion layer mobility in lateral MOSFETs when standard wet and dry oxidation processes are used. Afanas'ev et al studied NO and N₂O nitrided oxides on 4H-SiC and the effects on fast and slow interface traps [20]. They found that fast interface traps were reduced over the entire energy gap in both cases, due to removal of carbon clusters, as seen in Fig 7.

Fig. 7. Energy distribution of 4H-SiC/SiO₂ interface states obtained from ac conductance measurements on samples with oxides grown at 1300°C in dry O₂ (o) or 10% N₂O (■), and at 1175°C in NO (Δ) [20].

The major effect of NO-nitridation was seen to be the reduction in very slow traps in the oxide near the interface. Fig. 8 shows this result as a shift in the flat-band voltage of a MOS capacitor after being held in strong accumulation [20].

Fig. 8. Shift of the flatband voltage observed when lowering the temperature from 300 to 77 K in the n-type 4H-SiC MOS capacitors with ≈20-nm thick oxides grown at 1300 °C in dry O₂ (O) or in O₂+10%N₂O (□), and at 1175 °C in NO (Δ) as a function of maximum accumulation electric field strength. The V_{FB} values were taken when sweeping the voltage from accumulation to depletion [20].

This is in agreement with the results of a separate study using the slow trap profiling technique to measure traps with slow response times [21]. Fig. 9 compares wet and NO-nitrided oxides, with the wet oxide having a band of slow traps at around 0.2 eV below the 4H-SiC conduction band as evidenced by a broad, slow response peak at 0 volts, while in the nitrided case these are not evident.

Fig. 9. Slow Trap Profiles of (a) wet oxide and (b) NO-annealed dry oxide on 4H-SiC. The slow response peak around 0V in (a) is due to near interface traps located at 0.2eV below the conduction band edge [21].

CHARACTERISTICS OF MOS DEVICES

Many studies have shown that nitrided gate oxides produce superior MOSFET characteristics, such as lower on resistance as a consequence of improved channel mobility, higher gate breakdown voltages, and more practical threshold voltages. In the case of inversion-type MOSFETs on 4H-SiC, Das et al showed that NO-nitridation resulted in a four fold decrease in both fixed oxide charge and interface traps in the nitrided oxide compared to a dry oxidation followed by a low temperature wet anneal, as seen in Fig. 10 [22]. The nitridation process produced a low field electron mobility of $28 \text{ cm}^2/\text{Vs}$, was uniform across the wafer, independent of channel orientation in the c-plane, and only slightly reduced due to the presence of an ion implanted p-well.

Fig. 10. Capacitance-Voltage measurements on (a) 'Dry-Wet' MOSFET and (b) 'NO' MOSFET showing the reduced interface charges and trapping due to the post-oxidation NO annealing [22].

The output characteristic of a 4H-SiC enhancement mode n-channel MOSFET fabricated by Schorner et al with a NO-nitrided gate oxide are shown in Fig. 11[13]. The transfer characteristics appear in Fig. 12, and from this were extracted values for low field mobility of 48 cm²/Vs, and threshold voltage of 0.6V[13].

Fig. 11. Output characteristic of a 4H-SiC enhancement mode n-channel MOSFET with a designed length of 5 μm (substrate doping $N_A-N_D=6 \times 10^{14} \text{ cm}^{-3}$) [13].

Fig. 12. (a) Transfer characteristics of the 4H-SiC enhancement-mode n-channel MOSFET and (b) the corresponding transconductance [13].

Similar result was obtained by Chung et al in a study of NO-annealing of various gate oxidation processes on 4H-SiC [23][24]. The nitridation process resulted in an eight fold decrease in interface traps near the conduction band edge and a ten fold increase in field effect channel mobility to a value of $35 \text{ cm}^2/\text{Vs}$. Nitridation was also seen to produce a lower temperature dependence of the field effect mobility and a significantly reduced threshold voltage shift at higher temperatures.

Another problem affecting the long term stability of MOSFETs has been the barrier height lowering seen at the oxide-SiC interface. Yet it has been shown that NO annealed oxides produce electron injection barrier heights close to the theoretical value [25].

As well as MOSFETs for power and high frequency applications, the idea of using SiC MOS capacitors as charge-storage elements in nonvolatile memory devices has been investigated. In standard silicon memory, the deep-depletion capacitance level can be defined as the logic 1 level, whereas the inversion capacitance level can be defined as the logic 0 level. Given that the inversion capacitance is the value in thermal equilibrium, the charge-retention time of a MOS capacitor used as a memory element is determined by how long it takes for the capacitance to change from the deep depletion to the inversion state. Because of the wide bandgap the thermal generation process in SiC is extremely slow. Consequently, it should be possible to achieve very long charge-retention times at room temperature. In order to accelerate the thermal generation process, measurements were conducted at high temperature, and charge-retention times at room temperature extracted from an Arrhenius-type temperature dependence plot [26]-[28].

It was demonstrated that MOS capacitors with thermally grown dry oxides prevent their use as memory elements due to charge leakage through the gate oxide and poor quality of the passivating oxide-SiC interface that facilitates fast surface generation [27]. Due to these issues, the first SiC-based nonvolatile memory element was fabricated in an *n-p-n* structure [29]-[30]. By using a nitrided SiO_2 -SiC interface, both the charge leakage and carrier-generation rate can be reduced to an acceptable level. Fig. 13 shows charge-retention times using MOS capacitors on 4H- and 6H-SiC produced by two different nitridation techniques, i.e. *sandwich* process (100% NO/dry O_2 /100%NO) and high-temperature diluted- N_2O process. In the case of 4H-SiC, room temperature retention times were 1.49×10^{10} years for the *sandwich* process and 1.5×10^9 years for the dilute N_2O process. The *sandwich* process on 6H-SiC produced a lower value of 8×10^5 years. As these results illustrate, the charge-retention time is strongly affected by the interface-trap density (D_{it}), where the mid-gap interface traps are the most active.

Fig. 13. Arrhenius plots for charge-retention time for MOS capacitors on 4H- and 6H-SiC as a function of temperature for gate oxides grown in different processes. 4H-SiC, *sandwich* process, (τ); 4H-SiC, high temperature 10%NO, (O); 6H-SiC, *sandwich* process, ($\square$).

Another major benefit of an improved interface and oxide quality through nitridation is the improved reliability and long term stability of devices. Li demonstrated a dramatic improvement in the immunity of NO-nitrided oxides to high-field stress and high temperature negative-bias stress compared to inert gas annealed oxides [32]. N_2O nitridation was shown to produce similar benefits, even when diluted 10% in nitrogen [1]. Figure 14 compares the flatband voltage shift of a dry oxide to that of oxides grown or annealed in N_2O of various dilutions. An oxide grown in 10% N_2O at 1175°C was shown to have the best immunity to high-field stress.

Fig. 14. Flatband shifts during high-field stressing of oxide samples related to the N₂O process optimization: dry oxides (DRY-1100) annealed in either 10% (10% N₂O-A-1100), 20% (20% N₂O-A-1100) or 100% N₂O (N₂O-A-1100), dry oxides annealed at higher temperatures, 1150°C (N₂O-A-1150) and 1175°C (N₂O-A-1175), and oxide grown directly in 10% N₂O at 1175°C for 6 hours (10%-N₂O-G-1175) [1].

CONCLUSION

There is a growing body of evidence that many of the problems associated with producing high quality oxides on SiC can be overcome through various nitridation techniques. Oxide growth or annealing in the presence of nitric oxide appears to be the most effective method to enhance carbon removal and incorporate nitrogen at the interface, thereby lowering interface trap densities and improving dielectric strength and reliability. This in turn translates to improved low-field mobility and lower threshold voltages in MOSFET devices. While NO may not be the best option for industry, the more benign N₂O or diluted N₂O can also be used to produce device quality gate oxides.

In addition to the extensive work being done on SiC MOSFET development, investigations have begun on using the very desirable properties of SiC in charge storage devices for future non-volatile memory. To date, nitrided oxides on SiC show charge retention times far exceeding currently available silicon technology.

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