Selection of SPICE Parameters and Equations for Effective Simulation of Circuits with 4H-SiC Power MOSFETs

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Abstract. Power MOSFETs based on 4H-SiC have recently been commercialized and so circuit designers require SPICE models for simulation purposes in a range of applications including switch-mode power supplies. We present a selection of SPICE LEVEL 3 parameters and equations that can be used for effective circuit simulation of these MOSFETs, taking into account their unique characteristics for both static and dynamic operation.

Introduction

MOSFETs based on 4H-SiC have recently been commercialized for use in a range of applications including switch-mode power supplies for power conversion. Circuit designers use SPICE as the main tool to simulate devices in circuits such as those used in switch-mode power supplies. There are many sets of MOSFET equations in SPICE, called LEVELs with a huge number of equation parameters that can be used to simulate MOSFETs for a variety of different applications, ranging from power applications to CMOS microprocessors. A number of groups have studied both real and simulated devices and examined how well SPICE models fit the characteristics of 4H-SiC power MOSFETs. A 10kV DMOSFET was measured and simulated using a SPICE LEVEL1 model adapted to include temperature effects [1,2]. A vertical double implanted MOSFET structure has also been simulated and a SPICE model derived to match the results [3], and a more complex parameter extraction was applied in order to compare a 4H-SiC DiMOSFET with a Si power MOSFET [4].

It is difficult to select the most effective set of equations and especially the specific parameters that could be used for the simulation of circuits with 4H-SiC MOSFETs. This is so because the current-voltage characteristics of SiC MOSFETs have some unique features that differentiate it from Si MOSFETs, in particular the slow and nonlinear drain current increase with gate voltage which makes it difficult to define the threshold voltage. In this paper, we present the selection of a set of SPICE LEVEL 3 parameters that can provide effective simulation of circuits using 4H-SiC power MOSFETs.

SPICE Modeling and Parameter Extraction

Two commercially available 4H-SiC power MOSFETs were used in this study. MOSFET A is rated at 1200V and 35A, while MOSFET B at 1200V and 42A. Current-voltage and 1MHz capacitance-voltage characteristics were measured using an Agilent B1505 parameter analyzer.

Static Parameters. The selected static parameters needed to simulate the DC current-voltage characteristic are shown in Table 1 along with their respective units.

Table 1. Static Parameters

Spice keyword	Name	Units
LEVEL=3		
L	Gate length	m
W	Gate width	m
Vto	Zero bias threshold voltage	V
KP	Transconductance parameter	A/V ²
THETA	Mobility modulation constant	V ⁻¹
Tox	Gate oxide thickness	m
NFS	Subthreshold-current fitting parameter	cm ⁻² V ⁻¹

To enable the values of these parameters to be determined for specific 4H-SiC MOSFETs, the equations that define these parameters are as follows, presented in two segments.

$$V_{GS} > V_{TS}, \text{ where} \quad (1)$$

$$\text{and} \quad \text{---} \quad (2)$$

$$\left(\frac{I_D}{I_{D0}} \right) = \frac{1}{1 + \left(\frac{V_{GS} - V_{TS}}{V_{TS}} \right)^2} \left(\frac{V_{GS} - V_{TS}}{V_{TS}} \right) \quad (3)$$

$$V_{GS} < V_{TS}, \quad \left| \frac{I_D}{I_{D0}} \right| = \left[\frac{V_{TS} - V_{GS}}{V_{TS}} \right] \quad (4)$$

In Eqs. 1-4, V_{GS} is the gate-source voltage, V_t is the thermal voltage, q is the electron charge, ϵ_{ox} is the permittivity of the gate oxide, I_D is the drain current, and V_{DS} is the drain-source voltage. The selected parameters relate to the transfer current-voltage characteristic for small V_{DS} voltages only (output characteristics for higher V_{DS} were ignored), because power MOSFETs are used as switches where the ON mode corresponds to high V_{GS} and small V_{DS} , and the OFF mode corresponds to sub-threshold V_{GS} (small current). The equation for sub-threshold current (I_D for $V_{GS} < V_{TS}$) accounts for the slow and nonlinear drain current increase with gate voltage.. The parameter that is needed to model this effect is **NFS**. For the default case of **NFS**=0, $n_s=1$ and the subthreshold swing is equal the theoretical minimum $V_{TS}-V_{GS}=n_s V_t$ $\ln I_D=60$ mV/decade. In the case of these MOSFETs, however, the value of n_s is as high as 85.5, which corresponds to a subthreshold swing of 5.1 V/decade. The very high values of the **NFS** parameter relate to the high densities of near-interface traps in these MOSFETs, which cause the slow drain current increase with gate voltage.

In Figs. 1(a) and (b), the measured (line) and simulated (circles) transfer characteristics (I_D - V_{GS}) of the two commercial 4H-SiC MOSFETs are plotted, with the SPICE parameters used to generate the simulated data also listed on the figure. Following an assumption for the values of the technological parameters **L**, **W**, and **Tox**, fitting was achieved using the Marquardt-Levenberg algorithm which minimizes the sum of the squared differences between the measured and predicted values. These results demonstrate that a good fit can be achieved by this set of parameters, including the slow and non-linear rise in drain current with gate voltage in the subthreshold region.

Fig. 1. Measured (line) and simulated (circles) transfer characteristics of commercial MOSFET A, (a) and MOSFET B, (b). SPICE parameters used in Eqs. 1-4 to generate simulated data are listed.

Dynamic Parameters. In addition to the static parameters, dynamic parameters are necessary to enable meaningful simulation of the circuit time responses. These parameters relate to parasitic capacitances and they have to be specified to avoid the use of zero-default values by SPICE. The selected dynamic parameters are shown in Table 2.

Table 2. Dynamic Parameters

Spice keyword	Name	Units
Cgso	Gate-source overlap capacitance per gate width	F/m
Cgdo	Gate-drain overlap capacitance per gate width	F/m
Cjo	Zero bias capacitance	F
PB	Built-in voltage	V
Mj	Grading coefficient	-

The equations that define these parameters are as follows:

$$\left(\frac{C_g}{C_{db}} \right) \left(\frac{V_{db}}{V_{to}} \right) \quad (5)$$

$$\left(\frac{C_g}{C_{db}} \right) \left(\frac{V_{db}}{V_{to}} \right) \quad (6)$$

where C_g is the gate capacitance, C_{db} is the drain-body capacitance, and V_{db} is the drain-body voltage. The selected dynamic parameters and equations provide models for the gate-to-source and gate-to-drain capacitances (Eq. 5), and the voltage-dependent drain-to-body capacitance of the drain-to-body P-N junction (Eq. 6).

Figure 2 shows the measured and simulated plots of gate capacitance as a function of gate-body voltage for the two MOSFETs. There are complex dependencies of the gate capacitance on voltage, but they are not very significant, so the most effective way to model these capacitances is to use constant gate-to-source and gate-to-drain overlap capacitances per unit width (**Cgso** and **Cgdo** in SPICE).

Fig 2. Measured (line) and simulated (circles) C_g - V_{gb} plots for commercial MOSFET A, (a) and MOSFET B, (b). SPICE parameters used in Eq. 5 to generate the simulated data are listed.

The selected parameters for the drain-to-body capacitance (C_{db}) model the voltage dependence of the drain-to-body P-N junction using Eq. 6, as shown in Fig. 3 for the two MOSFETs

Fig 3. Measured (line) and simulated (circles) C_{db} - V_{db} plots for commercial MOSFET A, (a) and MOSFET B, (b). SPICE parameters used in Eq. 6 to generate simulated data are listed.

In conclusion, a simple set of SPICE LEVEL 3 parameters have been selected to enable effective simulation of circuits with 4H-SiC power MOSFETs. It has been demonstrated that these parameters and the related SPICE equations provide good fitting to two different commercially available 4H-SiC power MOSFETs.

References

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