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MOS Capacitor Characteristics of 3C-SiC Films Deposited on Si Substrates at 1270°C

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ABSTRACT

SiC films were deposited on Si substrate by low pressure hot-wall CVD using C₃H₈ (5% in H₂)-SiH₄ (2.5% in H₂)-H₂ gas system at 1270°C and 1370°C. MOS capacitors were fabricated on the grown 3C-SiC films. In this paper, we compare the electrical characteristics of MOS capacitors fabricated on 3C-SiC films deposited at high and low temperatures, 1370°C and 1270°C, respectively. The cross-sectional TEM images indicate similar SiC/Si interface microstructural quality for 3C-SiC films deposited at different temperatures, though a quicker elimination rate of stacking fault with increasing thickness at 1370°C, and rocking curves from XRD measurements indicate better crystalline perfection at 1370°C. The average surface roughness measurements performed by an atomic force microscope show that the surface roughness increases with elevated deposition temperature. The MOS capacitors were characterized by high-frequency capacitance-voltage (HFCV), conductance-voltage (G-V), and current-voltage (I-V) measurements at room temperature. The MOS capacitors fabricated on both films exhibit good and almost identical C-V characteristics. Measurements of current-voltage characteristics in accumulation region showed smaller leakage for the film deposited at 1270°C. It is concluded that the decrease of the deposition temperature from 1370°C to 1270°C does not bring any remarkable negative impact on the interface properties of fabricated MOS capacitors.

INTRODUCTION

The limitation imposed by Si and GaAs devices able to operate under extreme conditions has encouraged some research groups to investigate other semiconductors with wider energy gap. Hetero-epitaxial growth of 3C SiC films on silicon substrate has been attracting increasing attention [1, 2] because SiC-based devices can be integrated with the mainstream Si devices showing great potential in both electronic and micro/nano-mechanical applications. The conventional technique of deposition of 3C SiC films on silicon substrate is chemical vapour deposition (CVD) using separate precursors such as SiH₄ as Si source and C₃H₈ as carbon source [3]. There is a report showing that the best crystal quality and purity is usually obtained at relatively high temperature around 1350°C to 1400 °C for the deposition on Si substrate [4]. Ciobanu et al published a paper about the traps at the interface of 3C-SiC/SiO₂ MOS capacitor, in which the 3C-SiC film was deposited homoepitaxially by CVD at 1600 °C [5].

Heteroepitaxially grown 3C-SiC films on Si substrates by hot-wall CVD at 1370°C and 1270°C were used for the analysis presented in this paper. The electrical characteristics of metal-oxide-semiconductor (MOS) capacitors fabricated on these films were analyzed to investigate the influence of deposition temperature.
EXPERIMENT

SiC films were deposited on Si substrates using C$_3$H$_8$ (5% in H$_2$)-SiH$_4$ (2.5% in H$_2$)-H$_2$ gas system at 1270°C and 1370°C in a low pressure hot-wall CVD reactor. A detailed description of the CVD-system was already published elsewhere [6]. Ultra pure H$_2$ was used as the carrier gas, and the deposition of 3C-SiC films took place with the total pressure in the reactor of 150 mbar. MOS capacitors were fabricated on grown 3C-SiC films using the following process. The bare 3C-SiC/Si wafers were first cleaned in a mixture of H$_2$SO$_4$ and H$_2$O$_2$, followed by an RCA clean. This was then followed by 1% HF dip for 1 min. For better SiC/SiO$_2$ interface quality, the gate oxide layers were grown in 100% NO at 1160°C [5]. After that aluminum was thermally evaporated to form the gate electrodes and square capacitors with area of 0.0025 cm$^2$ were then defined by photolithography. The MOS capacitors were characterized by high-frequency capacitance-voltage (HFCV), conductance-voltage ($G$-$V$) and current-voltage ($I$-$V$) measurements at room temperature. The HFCV measurements were performed at the sweep rate of 0.1 V/s and the sweep range from 2V to -14V, using a computer-controlled HP4284A LCR meter. The $I$-$V$ measurements were performed at the sweep rate of 0.1 V/s and the sweep range from 0V to 15V, using a computer-controlled HP4145 meter. All the measurements were performed under light-tight and electrically-shielded conditions. The electrical analysis was complemented by transmission electron microscopy, high resolution X-ray diffraction (HRXRD) rocking curve and atomic-force microscopy to obtain information on structural characteristics and average surface roughness of the deposited 3C-SiC films.

RESULTS AND DISCUSSION

It is usually believed that higher temperature helps to improve the film quality. The full-width at half-maximum (FWHM) of 3C-SiC (002) HRXRD rocking curve decreases from 670 arcsec for sample A (deposited at 1270°C, 4.6 µm) to 380 arcsec for sample B (deposited at 1370°C, 4.9 µm), as shown in figure 1. The cross-sectional TEM images indicate similar SiC/Si interface micro-structural quality for both samples (shown in figure 2), while sample B shows a quicker elimination rate of stacking fault with increasing thickness than sample A. No etch pits are observed in either sample. All these results indicate a better crystalline quality at higher deposition temperature.

![Figure 1](image-url) 3C-SiC (002) HRXRD rocking curves of sample A (deposited at 1270°C) and sample B (deposited at 1370°C)
Figure 2 TEM micrographs of SiC films deposited at 1270 °C (a, c, e, for sample A) and 1370 °C (b, d, f, for sample B).
The average surface roughness (Ra) measurements performed by an atomic force microscope show that the Ra increases with elevated deposition temperature, from 10.8 nm for sample A to 34 nm for sample B. A smoother surface is preferred for improving device performance.

The MOS capacitors fabricated on both samples exhibit good and almost identical C-V characteristics (shown in Figures 3 and 4). The gate-oxide thickness, determined from the accumulation capacitance, is 28.3 nm. According to the measured C-V curves, both samples are confirmed to be $n$-type conduction and when fitted to theoretical curves, electron concentrations of $7 \times 10^{15} \text{ cm}^{-3}$ (sample A) and $5 \times 10^{15} \text{ cm}^{-3}$ (sample B) were determined. Minimum distortion

![Figure 3](image3.png)

**Figure 3** High frequency C-V and G-V curves for the 3C-SiC film deposited at 1270 °C (sample A).

![Figure 4](image4.png)

**Figure 4** High frequency C-V and G-V curves for the 3C-SiC film deposited at 1370 °C (sample B).
and small stretch-out observed in the measured as compared to the theoretical C-V curves indicate low interface traps density at the SiO2/SiC interface [7]. Similar level of conductance peaks also indicates similar level of interface-trap density for SiC films deposited at different temperatures. The C-V curves display a negative flat-band voltage shift for both capacitors. The negative flat-band voltage indicates the traps at SiO2/SiC interface have an effective value of 2.05×10^{12} and 1.91×10^{12} electronic charges/cm² for samples A and B, respectively. These results show that good quality oxide can be grown on the SiC films that are deposited at lower temperature, compared to the conventional deposition temperature.

Current voltage measurements in the MOS capacitor accumulation region were also used to study the quality of the deposited SiC films on samples A and B. Typical current voltage characteristics of both samples are shown in Figure 5. A smaller leakage current is obtained for sample A, deposited at 1270°C. This agrees well with the average surface roughness measurement results as the gate leakage current is affected by surface roughness, a smoother SiC surface makes a smoother SiC/SiO2 interface and SiO2 surface, and thus a smaller leakage current. It is possible that for the MOS capacitor the surface roughness plays a more important role than the stacking fault density in the 3C-SiC films. The yield of the MOS capacitors fabricated on both of the films is about 85%.

![Figure 5 Current-voltage characteristics in the accumulation region for both samples](image)

**CONCLUSIONS**

In summary, decreasing the deposition temperature of 3C-SiC films on Si substrates from 1370°C to 1270°C does not bring any remarkable negative impact on the interface properties of fabricated MOS capacitors, though the deposited 3C-SiC film has lower stacking fault density at 1370°C. Gate oxide grown by the NO process can form a high quality SiO2/SiC interface on SiC films deposited at different temperatures. Current voltage measurement indicated smaller leakage current for the SiC film deposited at 1270°C. It is possible that for the MOS capacitor the surface roughness of SiC film plays a more important role than the stacking fault density in the deposited 3C-SiC film. It is practical to deposit MOS capacitor quality 3C-SiC films at 1270°C on Si substrates.
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REFERENCES