Active Defects in 4H–SiC MOS Devices

Author

Haasmann, Daniel Erwin

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DANIEL ERWIN HAASMANN
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To my mum, dad and sisters

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Daniel Haasmann

STATEMENT OF ORIGINALITY

This work has not previously been submitted for a degree or diploma in any university. To the best of my knowledge and belief, the thesis contains no material previously published or written by another person except where due reference is made in the thesis itself.

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SELECTED LIST OF SYMBOLS

A..... Cross-sectional area

C..... Capacitance

C_A ..... Accumulation layer capacitance

C_{FB}..... Flat-band capacitance

C_{HF} ..... High-frequency capacitance

C_I..... Inversion layer capacitance

C_{LF}..... Low-frequency capacitance

C_P ..... Parallel capacitance

C_d ..... Depletion layer capacitance

C_{it} ..... Interface trap capacitance

C_m..... Measured capacitance

C_{ox} ..... Gate oxide capacitance

C_s..... Semiconductor capacitance

D_{it}..... Interface trap density

E_C ..... Conduction band edge

E_F..... Semiconductor Fermi-level

E_{FM} ..... Gate metal Fermi-level

E_{ox} ..... Gate oxide electric field

E_T ..... Trap energy level

E_V ..... Valence band edge

E_{cr}..... Critical electric field

E_g..... Energy band gap

f..... Frequency

G..... Conductance

G_P ..... Parallel conductance

G_m..... Measured conductance

h ..... Plank's constant

I..... Current

I_D ..... Drain current

J..... Current density

kT..... Thermal voltage

L_D ..... Debye length

m_{SiC} ..... SiC effective electron mass

m_{ox} ..... Gate oxide effective electron mass

N_A..... Acceptor doping concentration

N_D..... Donor doping concentration

N_{NIT} ..... Number of near–interface traps

n_i ..... Intrinsic carrier concentration

Q ..... Charge

Q_A..... Accumulation layer charge

Q_D ..... Depletion layer charge

Q_G..... Gate charge

Q_I ..... Inversion layer charge density

Q_{it}..... Interface trapped charge

Q_s ..... Semiconductor charge

q ..... Electron charge

$q\phi_{ms}$ ..... Metal-semiconductor work-function difference

R_S..... Series resistance

R_{ch} ..... Inversion channel resistance

$R_{DS(on)}$..... Drain-to-source resistance

R_d..... Drift region resistance

R_{it} ..... Interface trap resistance

R_{on} ..... On-resistance

$R_{sp(on)}$..... Specific on-resistance

t_{ox} ..... Gate oxide thickness

V ..... Voltage

V_B ..... Blocking voltage

V_{DS} ..... Drain-to-source voltage

V_{FB} ..... Flat-band voltage

V_G ..... Applied gate voltage

V_{GS} ..... Gate-to-source voltage

V_{on} ..... On-state voltage

V_{off} ..... Off-state voltage

V_{ox} ..... Gate oxide voltage

V_T ..... Threshold voltage

W_{drift} ..... Drift region width

w_d ..... Depletion layer width

x ..... Distance

γ ..... Body factor

ε_{ox} ..... Gate oxide permittivity

ε_s ..... Semiconductor permittivity

μ_{ch} ..... Inversion channel carrier mobility

μ_n ..... Semiconductor bulk carrier mobility

ρ ..... Resistivity

σ ..... Capture cross section

ϕ_B ..... Effective barrier height

ϕ_F ..... Fermi potential

φ_s ..... Surface potential

χ_s ..... Electron affinity

ω ..... Angular frequency

τ_c ..... Capture time

τ_e ..... Emission time

τ_{it} ..... Interface trap response time

Selected List of Abbreviations

AC ..... Alternating current

BFOM ..... Baliga's figure of merit

BJT ..... Bipolar junction transistor

C..... Carbon

CCDLTS..... Constant-capacitance deep level transient spectroscopy

C–V ..... Capacitance–voltage

DC..... Direct current

DD ..... Deep-depletion

F–D ..... Fermi–Dirac

F–N ..... Fowler–Nordheim

GaN..... Gallium nitride

GTO ..... Gate turn-off thrysistor

G–V ..... Conductance–voltage

H ..... Hydrogen

HF ..... High-frequency

HVDC ..... High-voltage direct current

IGBT..... Insulated gate bipolar transistor

IPE ..... Internal photoemission

JFET ..... Junction field-effect transistor

L ..... Length

LF ..... Low-frequency

MOS..... Metal–oxide–semiconductor

MOSFET..... Metal–oxide–semiconductor field-effect transistor

N ..... Nitrogen

NIT..... Near-interface trap

NO ..... Nitric oxide

N_2O ..... Nitrous oxide

O_2 ..... Oxygen

POA ..... Post oxidation anneal

PST..... Photon stimulated electron tunneling

RCA..... Radio Corporation of America

SCR ..... Silicon controlled rectifier

SIMS..... Secondary ion mass spectroscopy

SRH..... Shockley-Read-Hall

Si ..... Silicon

SiC..... Silicon carbide

SiO_2..... Silicon dioxide

W ..... Width

XPS..... X-ray photoelectron spectroscopy

1

INTRODUCTION

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1.1 SIGNIFICANCE OF THE RESEARCH

Electricity is considered the ultimate energy source in terms of convenience. It is an essential commodity of modern society. However, the deceivingly clean, zero-emission image locally perceived by the consumer disguises the fact that electricity is largely generated by the conversion of fossil fuels such as coal, crude oil and natural gas in power plants worldwide. This process releases substantial amounts of carbon dioxide and other greenhouse gasses in the earth's atmosphere which contribute to global warming and long-term climate change. Consequently, this energy paradigm has provoked a global effort to reduce greenhouse gas emissions by curbing the worldwide consumption of electricity. In order to achieve this objective, it is essential

to further develop new strategies and technology to target electrical power losses and to enhance the efficiency of electricity distribution.

A vast percentage of globally generated electricity goes through some form of electrical power conversion to meet the requirements of almost all electronic systems. Electrical AC–DC, DC–AC, DC–DC and AC–AC conversions are realised by electronic circuits which rely on modern solid-state semiconductor power switches such as thyristors, bipolar junction transistors (BJTs), metal–oxide–semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistor (IGBTs) that are driven into either conductive or non-conductive states in a periodic manner. These conversions are essential for fabrication of battery chargers, power supplies, inverters, electronic light ballasts, motor drives and long distance, high-voltage DC (HVDC) electricity transmission systems. Ideally the conversion of electricity from one form to another will not consume any power and amount to a conversion efficiency of 100%. However, all practical convertors will exhibit power losses due to the non-ideal characteristics of the semiconductor power switches that they are based on. Therefore, enhancing the efficiency of these power switches has become paramount in an effort to considerably reduce the worldwide consumption of electricity and consequently, reduce harmful greenhouse gas emissions.

It is generally considered that the two fundamental characteristics of a semiconductor power switch are (1) the resistance of the device in the on-state (*on-resistance*), which determines the on-state power loss and also, the overall current rating of the device, and (2) the voltage that can be sustained across the device in the off-state (*blocking voltage*) [1]. Both parameters are interrelated to one another due to the dependence of the blocking voltage on the semiconductor material parameters and geometry of the lightly-doped side of the P–N junction (*drift region*) that all power devices are based upon. A thicker and lower doped drift region is required

to support higher blocking voltages, although this inevitably increases the on-resistance of the drift region. In bipolar devices, the resistance of the drift region can be reduced by injecting minority carriers from an alternate semiconductor layer to significantly enhance the conductivity of the drift region. However, this mechanism incurs a trade off against switching speed due to the injected carrier lifetime, which results in a characteristic "*tail current*" and corresponding switching losses, therefore limiting the practical operational switching frequency of the device [2]. The size and subsequent cost of the supporting filter components (transformers, inductors, and capacitors) required in power conversion circuits are inversely proportional to the operational switching frequency. Therefore, the switching characteristics of power switches are practically as important as the on-resistance and blocking voltage capability.

Given the trade-offs that exist in the fundamental characteristics of semiconductor power devices, the designer that has to choose an appropriate device structure that satisfies the system requirements while minimizing parasitic losses to achieve the highest efficiency. This task is further compounded by thermal management, cost and size considerations. Ideally, the on-state power dissipation should be minimized while the device is optimized for operation at high blocking voltages and high frequencies. These factors are governed by the device structure and ultimately, the basic material properties of the semiconductor substrate from which these devices are fabricated on.

Silicon (Si) has essentially held the monopoly as the basic semiconductor material ever since the beginning of the solid-state semiconductor power device era. It has provided the pathway for high power device solutions in terms of power output density for many decades; however it is generally considered that the material properties of silicon have been virtually exploited to theoretical limits. Therefore, it is envisioned

that new technology involving alternate semiconductor materials can hold several advantages that can penetrate a power semiconductor market currently dominated by Si.

1.2 MATERIAL ADVANTAGES OF SiC FOR POWER ELECTRONIC DEVICES

In the 1980's, Baliga performed a fundamental analysis relating the semiconductor material properties to the specific on-resistance ($R_{SP(on)}$) of the drift region [3]. It was established that the specific on-resistance of the drift region was inversely proportional to the bulk carrier mobility and inversely proportional to the third power of the semiconductor energy bandgap for a given blocking voltage capability. The strong cubic dependence on the bandgap consequently sparked great interest in wide–bandgap semiconductors such as silicon carbide (SiC), gallium nitride (GaN) and diamond. It was theoretically demonstrated that these semiconductors could reduce the specific on-resistance and thus, reduce on-state power losses by orders of magnitude in comparison to devices fabricated on silicon substrates [4, 5]. Silicon carbide emerged as a prominent forerunner among many wide–bandgap semiconductors due to the fact that it is the only compound semiconductor that can form a native, high quality silicon dioxide (SiO_2) insulation layer by thermal oxidation. This feature provides a substantial advantage as conventional silicon processing and fabrication techniques can be adapted to further develop insulated-gate power switches such as MOSFETs and IGBTs with higher blocking voltages and lower on-state losses. Driven by these key motivational factors, the development and fabrication of SiC power devices became viable with the commercial availability of high quality SiC wafers in 1990 [6].

Silicon carbide offers many material advantages that make it extremely attractive for the use in high-power, high-frequency and high-temperature semiconductor device applications. All these advantages stem from its basic tetrahedron structure with a Si-C bond length of 1.89 Å that provides a much greater atomic interaction in comparison to silicon, where the Si-Si bond length is 2.35 Å. The stacking sequence of these tetrahedrons determines the overall SiC crystal lattice structure. These lattice structures are typically referred to as polytypes [7]. A large number of silicon carbide polytypes are known to exist; however, it has been the availability and quality of single crystal wafers in 3C, 4H and 6H that has made them the most promising candidates for the fabrication of SiC power electronic devices [8]. A comparison of fundamental material properties for these favourable polytypes has been listed in Table 1.1.

As a direct consequence of the wide–bandgap, SiC devices can tolerate much higher operational temperatures that arise from power dissipation induced localised heating. This is principally due to the far greater thermal energy required to excite electrons from the valence to conduction band compared to Si. Therefore, SiC devices will exhibit much lower off-state leakage currents at any given temperature due to significantly lower thermal intrinsic carrier generation. Furthermore, the thermal conductivity of SiC substrates is three–to–five times higher than Si. Consequently, the thermal resistance encountered between the junction and device casing is greatly reduced, thus improving heat dissipation from the junction and further simplifying device cooling requirements to provide overall system size and cost benefits. For high-frequency operation, the saturated electron velocity is twice that of Si. This is beneficial for microwave type devices as high currents can be switched quite rapidly.

TABLE 1.1 Fundamental Material Properties of Silicon and Silicon Carbide at 300 K [5, 8, 9].

Material Property	Si	SiC		
		3C	4H	6H
Bandgap (eV)	1.1	2.4	3.3	3.0
Intrinsic carrier concentration (cm^{-3})	10^{10}	10^{-1}	10^{-7}	10^{-5}
Electron saturation velocity (10^7cm / s)	1.0	2.5	2.0	2.0
Electron mobility (cm^2 / Vs)	1200	$=$ 750	$=$ 800 $\perp$ 800	$=$ 60 $\perp$ 400
Hole mobility (cm^2 / Vs)	420	40	115	90
Relative dielectric constant	11.9		9.7	
Breakdown field (MV / cm)	0.4	1.5	3.0	3.2
Thermal conductivity (W / cm°C)	1.5		3-5	

$=$: parallel to c-axis.

$\perp$: perpendicular to c-axis.

Perhaps the most notable material parameter for high-power semiconductor devices is the breakdown field strength. This parameter defines the highest electrical field the material can support before catastrophic breakdown occurs. The breakdown field strength of SiC is much higher than Si for a given doping concentration. This allows a significant reduction of the drift region width required to support a desired blocking voltage. A thinner drift region will decrease the resistance of the drift region and correspond to lower overall device on-resistances and conduction losses. Combined with the potential to also lower the doping concentration it has been anticipated that the specific on-resistance in SiC based power devices will be over two orders of magnitude lower for a given blocking voltage in comparison to Si [5]. Considering that silicon based devices have practically reached their theoretical limits of performance imposed by material properties, these projected improvements represent a rather substantial advance in power device technology.

The 4H–SiC polytype is the preferred material as it exhibits the widest bandgap, highest carrier mobility and relatively high breakdown field strength among the common polytypes. Accordingly, 4H–SiC is projected to demonstrate the greatest reduction in device on-state resistance based on theoretical appraisals [3-5]. In addition, the near isotropic mobility of 4H–SiC particularly favours the fabrication of pre-existing vertical power device structures. Among many device structures, the SiC power MOSFET is expected to have the most prominent impact on the Si dominated power device application market. In particular, SiC MOSFETs are posed to replace Si IGBTs with sub 10 kV voltage ratings and possibly become competitive with Si gate turn-off thyristors (GTOs) of lower voltage ratings [10]. Silicon IGBTs are currently dominant in applications where device voltage ratings are between 1.2 kV and 6.5 kV [11]. However, the switching losses are relatively high in these devices since they rely on bipolar conduction, limiting the practical operational frequency and the overall efficiency, size and cost of the overall convertor. In comparison, SiC MOSFETs can offer greater system efficiency by considerably reducing parasitic power losses, particularly at high frequencies, and relax thermal management considerations by tolerating much higher operational temperatures. The significance of the 4H–SiC polytype in developing highly efficient SiC MOSFETs has been a major focus of research groups over the past decade. The potential impact of such a device provides the key motivational factor for the study presented in this thesis.

1.3 BENEFITS OF SiC POWER MOSFETs

Silicon based power MOSFETs have gained immense popularity since their introduction and have become the dominant semiconductor switch in many applications as a result of their excellent electrical characteristics and simplified drive requirements. However, the relatively low breakdown field of Si severely limits the maximum blocking voltage capability of the PN

junction which precludes the use of these devices in high voltage applications due to high on-resistances and ensuing conduction losses. This trade off can be reduced and the practical operational voltage increased by using semiconductors with superior material properties such as 4H–SiC.

A cross section of a typical N-channel vertical double-implanted power MOSFET (DMOSFET) structure is shown in Fig. 1.1. Once gate-to-source voltage is greater than the specified threshold voltage ($V_{GS} > V_T$), a low resistance inversion channel will form in the P-body region at the semiconductor-oxide interface, allowing current to flow from the drain to the source. In addition to the resistance associated with the channel (R_{ch}), the other major contributor to the overall on-resistance of the device is the resistance associated with the drift region (R_d). This is due to the fact that power MOSFETs require much thicker and lower doped drift regions to block relatively high voltages in the off-state compared to conventional low-voltage MOSFETs. Neglecting the relatively minor resistances associated with the JFET region and the contacts, the overall on-resistance in a vertical power MOSFET can be expressed by

$$R_{DS(on)} = R_{ch} + R_d \tag{1.1}$$

As the resistance of the drift region proportional to the blocking voltage capability of the device, it dictates the lower limit for the on-resistance in high voltage devices. Therefore the overall on-resistance of an ideal power MOSFET can be estimated by performing an analysis of the drift region to relate the drift resistance to the blocking voltage capability. Higher blocking voltages can be obtained by either decreasing doping concentration of the drift region or increasing the width of the drift region. However, both parameters inevitably increase the resistance of the drift region, resulting in higher device on-resistances [3]. These parameters must

therefore be optimized in order to realize the lowest possible on-resistance for a given blocking voltage.

In the off-state, whereby both the source and gate are grounded, the P–N junction formed by the P-body and N^- drift regions becomes reversed biased with respect to positive drain voltages. This junction entirely blocks the voltage at the drain by extending a depletion layer from both sides of the P-body into the N^- drift region. Applying additional drain voltage once the depletion layer edge has reached the highly doped N^+ substrate will rapidly increase the electric field strength in the semiconductor. When the induced electric field reaches the breakdown field strength of the semiconductor, a large uncontrollable current will be able to flow as a result of avalanche multiplication and will cause irreparable damage.

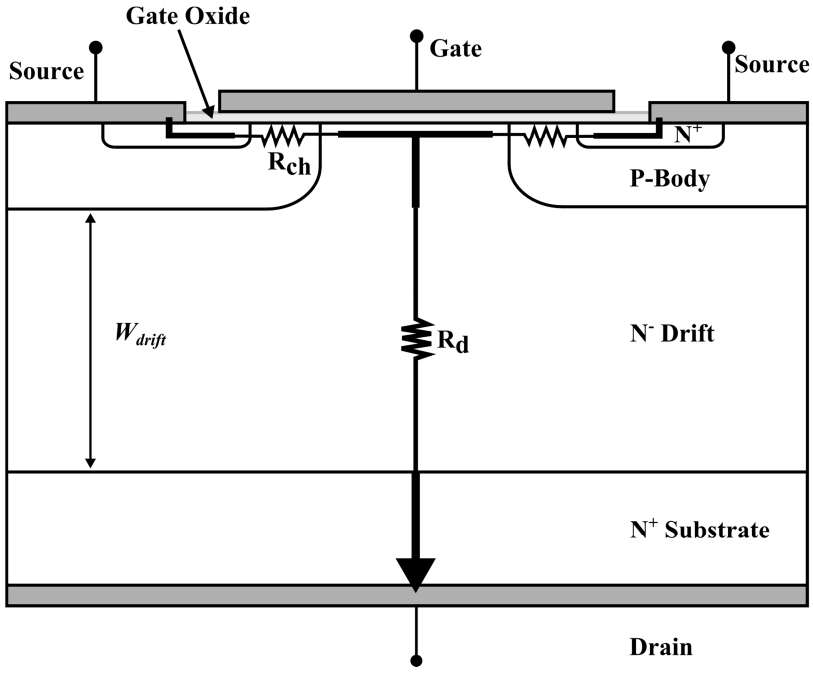

Figure 1.1 Cross sectional view of the current path and the main resistive elements in a typical DMOSFET structure.

The only way to achieve a higher blocking voltage capability for the critical electric field strength that can be supported by the material (E_{cr}) is to lower the doping concentration of the drift region (N_D) [1],

$$V_B = \frac{\varepsilon_s {E_{cr}}^2}{2qN_D} \tag{1.2}$$

provided that the width of the drift region (w_{drift}) is no less than the depletion layer width (w_d) at the desired blocking voltage,

$$w_{drift} \geq w_d = \sqrt{\frac{2\varepsilon_s V_B}{qN_D}} \tag{1.3}$$

where ε_s is the permittivity of the semiconductor and q is the electron charge. Therefore a thicker drift region is required to support a higher blocking voltage. However, increasing the width of the drift region also increases the *length* of the drift region resistor. Thus, the overall resistance of the drift is dependent on the width as well as the resistivity (ρ) and the cross-sectional area (A) of the drift region as given by the following expression:

$$R_d = \rho w_{drift} \frac{1}{A} \tag{1.4}$$

The technological parameter is the resistance per unit area or the specific on-resistance ($R_{SP(on)}$) of the drift region, where the area is the geometric design parameter. Given that $\rho = q\mu_n N_D$, the specific on-resistance of the drift can be determined by

$$R_{SP(on)} = R_d A = \frac{w_{drift}}{q\mu_n N_D} \tag{1.5}$$

With the optimal doping concentration and drift region width determined from Eqs. (1.2) and (1.3) respectively, the specific on-resistance of the drift region to support a desired blocking voltage becomes [12],

$$R_{SP(on)} = \frac{4{V_B}^2}{\mu_n \varepsilon_s {E_{cr}}^3} \tag{1.6}$$

where μ_n in Eqs. (1.5) and (1.6) is the carrier mobility in the semiconductor bulk.

This parameter represents the theoretical device on-resistance for a given area assuming the resistance of the drift dominates all other resistive sources. Since this relationship between the specific on-resistance and the blocking voltage only involves material properties it is particularly suitable for evaluating the merit of various semiconductor materials for power device applications. The denominator of the expression is known as Baliga's figure of merit (BFOM) which relates the semiconductor material parameters to the on-state conduction loss of the device due to the resistance of the drift region [3, 13]. The BFOM for 4H–SiC is over 500 times greater than Si using the material parameters outlined in Table 1.1. Therefore it can be anticipated that specific on-resistance of SiC power MOSFETs can be reduced by over two orders of magnitude for a given blocking voltage in comparison to Si-based counterparts.

The theoretical limits for the specific on-resistance as a function blocking voltage in silicon and 4H-SiC is illustrated in Fig. 1.2. This figure clearly highlights the material limitations imposed by the relativity low breakdown field strength of Si. The dominance of the drift region resistance in Si based power MOSFETs generally limits their practicality to blocking voltages below a few hundred volts. For applications requiring higher voltage ratings the circuit designer traditionally has to resort to bipolar devices that have much lower conduction losses at the expense of higher switching losses. There is no possible design or processing resolutions to alleviate this limit since the specific on-resistance of the drift region represents the fundamental limit imposed by material properties. However,

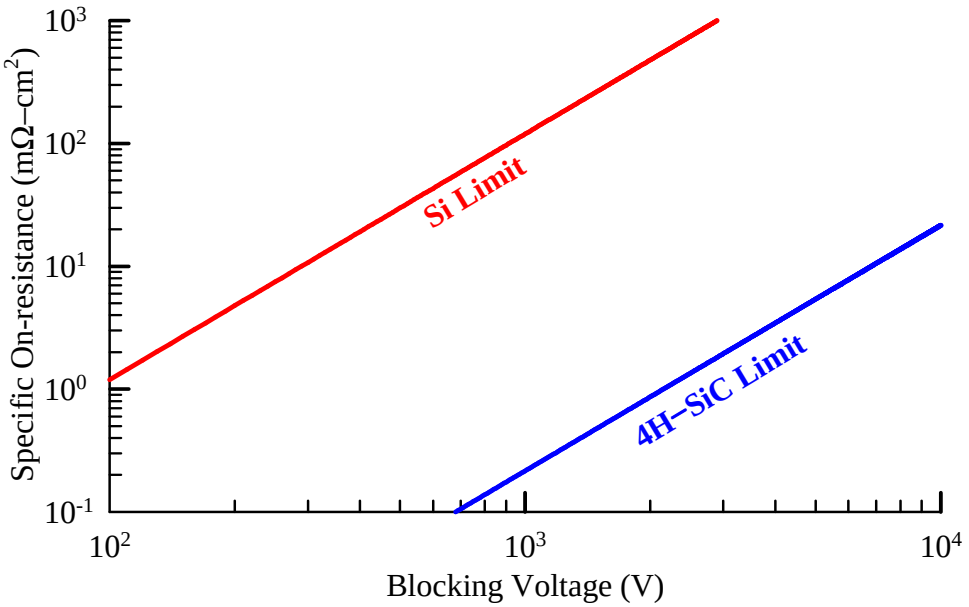

Figure 1.2 The theoretical specific on-resistance of the drift region as a function of blocking voltage capability as determined by the material properties of 4H–SiC and Si.

as demonstrated, SiC MOSFETs can theoretically surpass the specific on-resistance limit of Si by a large margin and therefore can significantly lower conduction losses while supporting blocking voltages in the range of several kV. Combined with inherently low switching losses, SiC MOSFETs have the potential to replace the current state-of-the-art Si-IGBTs and improve the overall efficiency of the power convertor design.

1.3.1 Current Status and Practical Challenges

The analysis conducted in the previous section has highlighted the tremendous potential of power MOSFETs fabricated on SiC. Based on the specific on-resistance of the drift region, high-voltage SiC MOSFETs are expected to reduce conduction losses by a considerable margin compared to the same devices fabricated on Si. In addition, the ability to thermally grow

SiO_2 as a gate dielectric has been a key motivational factor to pursue the development of SiC power MOSFETs. However, early attempts to fabricate these devices by adopting standard silicon processing technology resulted in extremely poor electrical characteristics and far greater on-resistances than theoretically expected [14-16]. It became apparent that the resistance of the drift region was no longer the dominant factor and that the very high on-resistance in kV-rated SiC MOSFETs was instead, dominated by excessive inversion channel resistance [17].

The channel resistance is typically obtained from the linear region of the $I_D - V_{DS}$ output characteristics where the MOSFET is *on* and operates as a voltage-controlled resistor, which is modulated by the applied gate voltage. In the *linear* mode of operation the current through the channel can be modelled by the following equation:

$$I_D = \frac{W}{L}\,\mu_{ch} C_{ox}(V_{GS} - V_T)V_{DS} \tag{1.7}$$

The resistance of the channel is then,

$$R_{ch} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_{ch} C_{ox}(V_{GS} - V_T)}\frac{L}{W} \tag{1.8}$$

where L and W are the effective length and width of the inversion channel, μ_{ch} is the average electron mobility in the inversion channel, C_{ox} is the gate oxide capacitance per unit area and V_{DS}, V_{GS} and V_T are the drain-to-source, gate-to-source and the threshold voltage respectively. The inversion layer charge density ($Q_I = C_{ox}(V_{GS} - V_T)$) is proportional to the applied gate voltage once above the threshold voltage, and zero below. Given the L/W design parameter is limited by practical cell packing density constraints, the high channel resistance observed in SiC MOSFETs becomes dependent on the factors that influence carrier (electron) concentration in the inversion channel, given by Q_I/q, and the mobility of these channel electrons. These

parameters are directly influenced by the critical nature of the gate oxide and the oxide–semiconductor interface. In the case of modern Si technology, the inherent quality of the Si–SiO_2 interface obtained by standard thermal oxidation procedures has proven sufficient for the facilitation of high performance Si MOS devices. On the other hand, the electronic passivation of the SiC–SiO_2 interface formed by standard thermal oxidation is quite ineffective, leading to a high density of electrically active interfacial defects. These defects fundamentally *trap* a large number of inversion channel electrons and reduce the actual mobility of the remaining free carriers due to scattering [18]. Combined, these factors significantly impede the conductance of the inversion channel which has been evident in the extremely low channel-carrier mobilities that is commonly reported in SiC MOSFETs with conventional thermally grown dry or wet gate oxide, particularly on 4H [19, 20].

Attempts to enhance the quality of the SiC–SiO_2 interface by hydrogen annealing and passivation that are highly effective in Si technology proved futile, suggesting that the source of the inferior interface quality on SiC was very different to that of the well-known Si–SiO_2 interface. The fundamental differences between the two systems has been commonly attributed to the complex oxidation kinetics that led to carbon clustering and suboxide bonding at the interface [21], in addition to the inherently wider bandgap of SiC that could encompass defects of energy levels otherwise inactive in Si [22].

For over a decade, the quality of the 4H–SiC/SiO_2 interface remained the fundamental roadblock in the development of device-quality SiC MOSFETs. However, it was eventually discovered that nitridation of the SiC–SiO_2 interface by either post oxidation annealing (POA) or direct growth in nitric oxide (NO) or nitrous oxide (N_2O) could significantly improve the electrical properties of the interface [23, 24] and enhance the

inversion channel-carrier mobility to acceptable levels [20, 25, 26]. This breakthrough revived the interest in SiC–MOSFETs which finally enabled the development of commercial devices that are currently available from companies such as Rohm and CREE. The latest offering from Cree Inc. demonstrates an overall on-state resistance of only 25 mΩ for a blocking voltage of 1.2 kV [27], which is significantly less than the on-resistance of competing Si-based MOSFETs of the same blocking voltage capability [28].

The transfer characteristic of a commercially available SiC MOSFET is shown in Fig. 1.3. It can be seen that the turning *on* of this MOSFET is gradual and that relatively high gate drive voltages of up to 25 V are required to achieve sufficient output currents. This problem still relates to issues of interface passivation, because a large fraction of the channel electrons are still being trapped by electrically active defects at and near the $SiC–SiO_2$ interface. These MOSFETs do provide a smaller on-resistance for a higher blocking voltage than the theoretical limit of Si and, accordingly they enable switch-mode power circuits with improved efficiency, and in combination with SiC Schottky diodes, significantly reduced size. Nonetheless, it is obvious from the transfer characteristic shown in Fig. 1.3, combined with the particularly low channel-carrier mobilities that are commonly reported, that significant advances are still theoretically possible and if the quality of $SiC–SiO_2$ interface is further improved, the performance of SiC MOSFETs will approach the theoretical limit of SiC (as illustrated in Fig. 1.2).

Enhancing the performance of these devices ultimately relies on the further development of gate oxide growth processes and surface passivation techniques to improve the quality of the $SiC–SiO_2$ interface. Integral to these developments is the ability to correctly characterize and evaluate the $SiC–SiO_2$ interface with respect to the electrically active defects that dominate the inversion channel-carrier mobility and thus, the channel

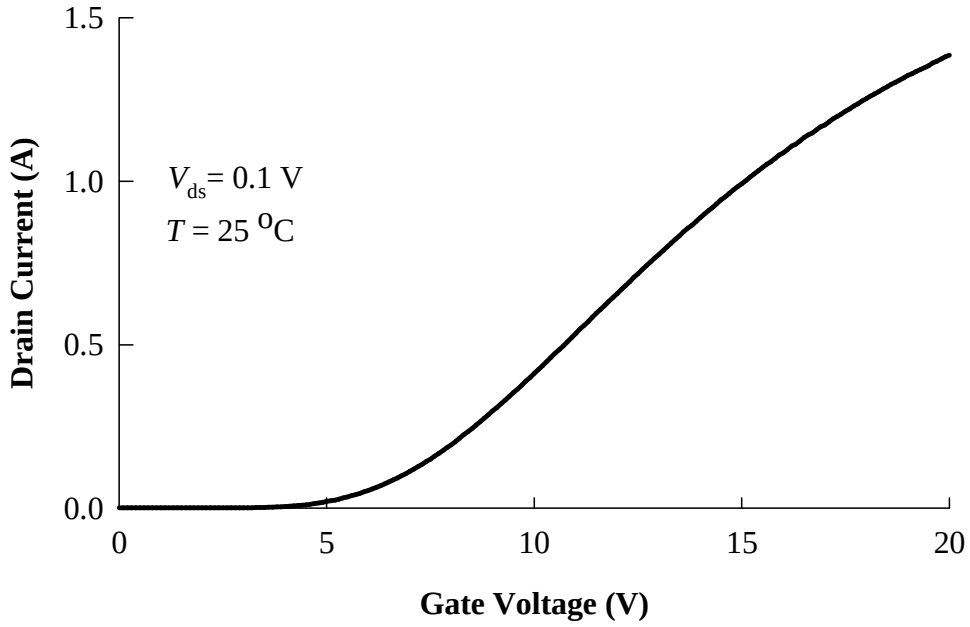

Figure 1.3 The transfer characteristic of a commercially available SiC power MOSFET [34].

resistance in SiC MOSFETs. Even though the native oxide of SiC is analogous to that of Si, the properties of the semiconductor-oxide interfaces are markedly different. Yet, a majority of the techniques employed to characterize the SiC MOS interface are directly borrowed from Si MOS technology developed as far back as the 1960's [29]. Using these techniques, the quality of the SiC–SiO_2 interface is typically characterized by the interface state (trap) density (D_{it}), which is conventionally estimated from measured admittance response of SiC MOS capacitors. Although, interpreting the D_{it} of the SiC–SiO_2 interface in terms of the inversion channel-carrier mobility in SiC MOSFETs has proven less straightforward than that of Si devices.

Currently, the D_{it} energetically located in close proximity to the 4H–SiC conduction band is of most interest to the SiC community because reducing the density of these defects has been accompanied by increased inversion channel-carrier mobility. They are considered to be near-interface

traps (NITs), spatially located in the oxide, due to their relatively high density and long response times [21, 30]. However, the validity of the generally accepted correlation between the density of NITs and the channel-carrier mobility in SiC MOSFETs seems debatable as several reports have indicated that it is not universally supported [31-33]. The reported inconsistencies could well stem from the fact that traditional Si-based MOS interface characterisation techniques were originally developed to estimate the density of conventional interface traps, spatially located at the semiconductor-oxide interface, with energy levels near the midgap of silicon [29]. In addition, it is also possible that there may be other factors, inherent to SiC–SiO_2 interface that degrade the inversion channel-carrier mobility in SiC MOSFETs and cannot be detected or examined by conventional MOS interface characterisation methods. This warrants further investigations to improve the understanding of the electrically active defects in 4H–SiC MOS devices.

1.4 THESIS OUTLINE

In light of the concerns highlighted in the previous section, this thesis is devoted to improving the understanding of the factors that degrade the inversion layer electron transport and impede the inversion channel-carrier mobility in 4H–SiC MOSFETs. The dominant defects are identified and a novel technique to detect these defects in MOS capacitors is proposed. To improve the quality of SiC–SiO_2 interfaces, two alternate gate oxide nitridation processes are proposed and experimentally verified. The general outline and key research areas of this thesis are described in greater detail in the following paragraphs.

Given the widely accepted use of silicon derived MOS interface characterisation techniques on SiC MOS structures, a review on the fundamental electrostatics of the MOS capacitor and the effects of interface traps is presented in **Chapter 2**. The theory behind the most common capacitance–voltage (C–V) and conductance–voltage (G–V) based techniques to extract the interface trap density is introduced to provide the necessary background knowledge for the following chapters.

Chapter 3 begins with a critical review on the present understanding of the defects at the SiC–SiO_2 interface in terms of their impact on the effective inversion channel-carrier mobility in 4H–SiC MOSFETs. Several discrepancies in the direct application of conventional MOS interface trap theory and characterisation techniques, outlined in the preceding chapter, to the SiC–SiO_2 interface are exposed, leading to a novel understanding of the electrically active defects that are directly responsible for the channel-carrier mobility degradation in 4H–SiC MOSFETs. With the near-interface traps energetically aligned to the conduction band identified as the electrically active defects responsible for the severe trapping of channel electrons from the inversion layer in SiC MOSFETs, a novel interface

characterisation technique to detect these defects, based on the accumulation conductance measurements of N-type 4H–SiC MOS capacitors, is proposed and experimentally demonstrated. In addition, the transfer mechanism between the NITs aligned to the conduction band and the free channel-carriers is experimentally verified.

With a better understanding of the dominant defects in 4H–SiC MOS devices, **Chapter 4** concentrates on the development of gate oxide growth processes. A brief review on the oxidation and the physical properties of the SiC–SiO_2 interface reveals that gate oxides thermally grown in 100% NO exhibit the best SiC–SiO_2 interface properties; however the extremely slow growth rate combined with the volume of the gas required in large production-based oxidation furnaces precludes the growth of thick oxides required for the fabrication of SiC power MOSFETs. To alleviate these issues, two alternative gate oxide nitridation processes are presented. A conventional *sandwich* ($NO/O_2/NO$) type process and a novel, combined O_2 and NO process both employing NO at an extremely low partial pressure of 2 % in a large volume oxidation furnace, representative of a production type environment, are investigated in terms of interface quality and oxide reliability. The new characterisation technique developed in the previous chapter is successfully applied to study effect of these processing conditions on the active near-interface traps aligned to the conduction band.

Finally, the key conclusions and developments made throughout the study along with recommendations for future work are summarized in **Chapter 5**.

1.5 ORIGINAL RESEARCH CONTRIBUTIONS

The original research contributions developed in this thesis can be summarised as follows:

- A critical analysis of the spatial and energetic positions of the interfacial defects in SiC MOS devices identifies short comings of conventional MOS characterisation techniques and theory applied to the SiC–SiO_2 interface.

- It is determined that the electrically active near-interface traps, directly responsible for the trapping of inversion layer electrons, are aligned to the conduction band.

- A novel technique, based on the measured conductance of 4H–SiC MOS capacitors in strong accumulation, to characterise the energy levels of the active near-interface traps aligned to the conduction band is proposed.

- An experimental demonstration confirms that the transportation mechanism between the active near-interface traps aligned to the conduction band and the mobile electrons is due to thermally independent tunnelling.

- A novel gate oxidation process combining O_2 and NO at low partial pressure to improve the SiC–SiO_2 interfacial properties whilst significantly reducing the amount of nitric oxide required for large, production type oxidation furnaces is proposed.

1.5.1 Related Publications

The analysis and key findings presented in the thesis has led to the following publications:

Journal Articles

D. Haasmann and S. Dimitrijev, "*Energy position of the active near-interface traps in metal-oxide-semiconductor field-effect transistors on 4H-SiC*", Applied Physics Letters, 103, 113506 (2013).

D. Haasmann, S. Dimitrijev, J. Han and A. Iacopi, "*Growth of Gate Oxides on 4H-SiC by NO at Low Partial Pressures*", Materials Science Forum, Vols. 778-780, pp 627-630 (2014).

H. A. Moghadam, S. Dimitrijev, J. Han, **D. Haasmann** and A. Aminbeidokhti, "*Transient-Current Method for Measurement of Active Near-Interface Oxide Traps in 4H-SiC MOS Capacitors and MOSFETs*", to be published.

Conference Articles

S. Dimitrijev, J. Han, **D. Haasmann**, H. A. Moghadam and A. Aminbeidokhti, "*Power-Switching Applications Beyond Silicon: The Status and Future Prospects of SiC and GaN Devices*", 29th International Conference on Microelectronics, Belgrade, Serbia, 12-14 May 2014.

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2

MOS Device Physics and Interface Characterisation Techniques

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2.1 INTRODUCTION

The electrical characteristics of all MOS based devices are strongly influenced by the physical and electrical properties of the oxide dielectric layer and the semiconductor-oxide interface. Oxidation of the semiconductor bulk gives rise to electrically active defects due to the inhomogeneity of the crystal lattice at the surface of the semiconductor. A number of these defects are located at or very near to the semiconductor-oxide interface. Given their very close proximity to the underlying semiconductor bulk they can effectively *trap* and release mobile holes and electrons. Because they can dynamically trap mobile charge carriers they are commonly referred to as *interface traps*. A high density of interface traps is known to adversely affect the operation of MOSFETs, including: the inefficient modulation of the inversion channel, as a result of the associated interface trapped charge, and the degradation of the effective channel-carrier mobility in the inversion channel, due to the trapping of mobile charge carriers. Consequently, methods capable of quantifying the interface trap density and the corresponding energy positions of the electrically active defects are crucial for the development of high-quality semiconductor-oxide interfaces required to facilitate practical applications of MOS structures.

For many decades, only the thermally oxidized silicon/silicon-dioxide ($Si–SiO_2$) system has been able to demonstrate device-quality interfaces. Owing to this dominance, the fundamental theory behind the operation of MOS devices and the techniques to electrically characterise the semiconductor-oxide interface are principally based on the behaviour of $Si–SiO_2$ MOS structures. Nonetheless, the theory and techniques are generally applicable to all oxide-semiconductor systems. Conventional silicon based MOS interface characterisation techniques are often universally adapted to examine the $SiC–SiO_2$ system, especially given that the thermal oxidation of

SiC yields a stoichiometric SiO_2 layer with a density, refractive index, dielectric constant and breakdown strength are analogous to that of thermal grown oxides on Si [1-3].

This chapter is devoted to the electrical characterisation of the MOS structure. A brief overview of the structure and fundamental theory behind the principle operation of a MOS capacitor is firstly introduced. This is then followed by a review of the most common techniques to quantitatively examine the non-ideal effects in MOS capacitors due to fixed oxide and interface trapped charge using capacitance–voltage and conductance–voltage measurements.

2.2 MOS CAPACITOR: STRUCTURE AND PRINCIPLE OF OPERATION

Combined with the relative ease of fabrication and the wealth of information regarding the quality of the oxide-semiconductor interface the MOS capacitor has naturally lent itself to becoming the most prominent MOS test structure. The critical processing steps concerning the thermal oxidation of the semiconductor surface and subsequent oxide-semiconductor interface are essentially identical to that of a MOSFET. Therefore the electrical measurements obtained from the characterisation MOS capacitor can provide valuable insight in determining the MOSFET characteristics aiding development time. It is possible to obtain equally accessible information of the semiconductor-dielectric interface from a large-area MOSFET test device although there are no advantages to be gained. In addition the transistor fabrication process itself may introduce superfluous issues leading to additional sources of error otherwise not found in MOS capacitors. The only benefit the MOSFET has over the MOS capacitor is that the inversion channel mobility and other critical parameters can be directly measured and the influence of interfacial and

oxide properties can be directly related to it [4]. This is of key importance for the correlation of the results obtained by MOS capacitor measurements.

The metal–oxide–semiconductor (MOS) capacitor is a simple two-terminal device, which traditionally consists of a thermally grown silicon dioxide (*oxide* for short) dielectric layer sandwiched in between a vacuum deposited *metal* or deposited polysilicon electrode and a silicon (*semiconductor*) substrate as shown in Fig. 2.1a. Metal is also deposited along the bottom of the structure to form an ohmic contact with the silicon substrate. This contact is generally referred to as the *body* while the metal or polysilicon electrode is called the *gate*. A voltage is typically applied to the gate (V_G) while the body is grounded.

The structure is virtually identical to that of a conventional parallel-plate metal–dielectric–metal capacitor with one metal electrode replaced by a semiconductor. However, unlike the fixed capacitance of a conventional

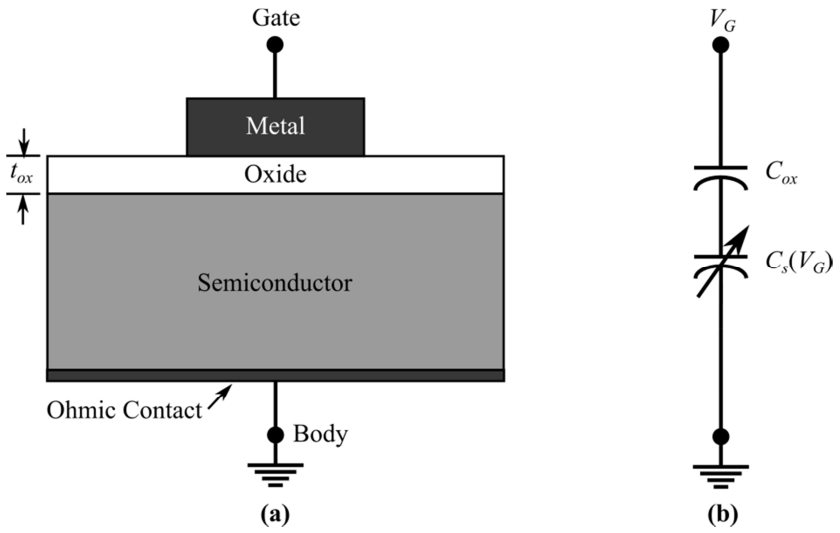

Figure 2.1 (a) Cross section and (b) simplified equivalent circuit model of an ideal MOS capacitor. The semiconductor capacitance (C_s) is shown variable to denote its dependence on the gate voltage (V_G).

capacitor, the capacitance of a MOS structure depends on the voltage that is applied to the gate with respect to the body. The equivalent circuit of an ideal MOS capacitor can be simply modelled by a variable semiconductor capacitance (C_s) in series with a fixed oxide capacitance (C_{ox}) as shown in Fig. 1.1b. The voltage dependant semiconductor capacitance results from the modulation of the surface region or depletion layer width of the semiconductor substrate that is induced by the electric field perpendicular to the gate electrode. Accordingly, the surface conductivity of the semiconductor is also modulated due to the varying distribution of charges in the semiconductor. This phenomenon is known as the *field effect* which underlies the operation of all MOS based devices [4].

There are three fundamental capacitance–voltage (C–V) characteristic modes of a MOS capacitor, namely: *accumulation*, *depletion* and *strong inversion*. These modes are defined by two boundary voltages: the *flat-band voltage* (V_{FB}) and the *threshold voltage* (V_T). For a MOS capacitor fabricated on a P-type substrate, the three characteristic modes of operation can be briefly described as follows [5]: (1) in accumulation, negative effective gate voltages ($V_G - V_{FB} < 0$) draws a high concentration of holes (majority carriers) to the surface of the semiconductor forming an accumulation layer at the semiconductor surface, (2) in depletion, small positive effective gate voltages ($V_G - V_{FB} > 0$) repel holes from the surface region forming a depletion layer, and (3) in strong inversion, large positive gate voltages ($V_G - V_T > 0$) attracts a high concentration of electrons (minority carriers) to surface of the semiconductor forming an inversion layer at the semiconductor surface. A typical capacitance–voltage curve of a P-type MOS capacitor highlighting these characteristic modes of operation is illustrated in Fig. 2.2. The behaviour of an N-type MOS capacitor is completely analogous to that of a P-type structure with the gate voltage mirrored about the flat-band voltage. This chapter will mainly focus on the P-type MOS capacitor as it governs the operation of N-channel MOSFETs.

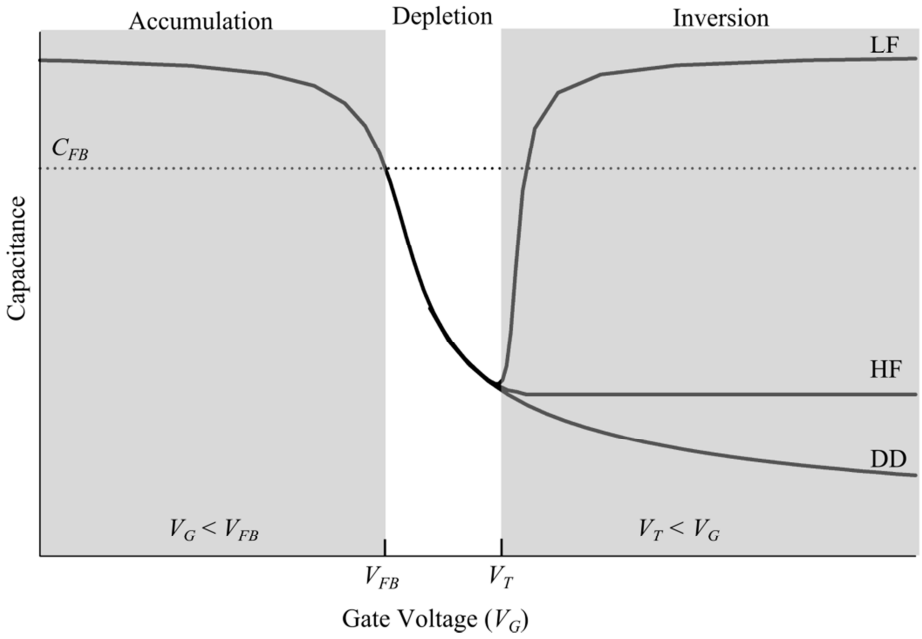

Figure 2.2 Typical low-frequency (LF), high-frequency (HF) and deep depletion (DD) capacitance–voltage (C–V) curves of a MOS capacitor on a P-type substrate illustrating the three characteristic modes of operation: accumulation, depletion and strong inversion. The flatband voltage (V_{FB}) separates the accumulation and depletion regions, while the threshold voltage (V_T) separates the depletion and strong inversion regions.

A practical approach to obtain the capacitance–voltage characteristics of a MOS capacitor is to apply a variable DC bias with a superimposed, small amplitude AC signal to the gate contact and measure the resulting current. By integrating the current over time the charge can be derived and the MOS capacitance at a given DC bias voltage can then be acquired as a result of charge variation provided by the small-signal AC bias. By definition, the capacitance relates an incremental change in voltage to a corresponding change in charge:

$$C \equiv \frac{\partial Q}{\partial V} \tag{2.1}$$

From the gate, the capacitance of a MOS capacitor can therefore be written as $C = \partial Q_G/\partial V_G$, where Q_G is the gate charge. To maintain charge neutrality in the system charge is induced in the semiconductor near its surface to counterbalance the charge at the gate, thus $Q_G = -(Q_s)$. The gate voltage is partially dropped across both the oxide and the semiconductor, yielding $V_G = V_{FB} + V_{ox} + \varphi_s$, where V_{ox} is the voltage across the oxide and φ_s is referred to as the semiconductor *surface potential*. The surface potential is defined as the potential difference between the semiconductor surface and semiconductor bulk. It is a crucial parameter in terms of understanding the operation of a MOS capacitor as it determines the surface carrier concentration in the semiconductor surface region. Combining the concept of charge neutrality and the gate voltage distribution in an ideal MOS structure, free of any built in fixed or interface charges, allows Eq. (2.1) to be written as [6]

$$C = -\frac{\partial Q_s}{\partial V_{ox} + d\varphi_s} \tag{2.2}$$

The semiconductor charge depends on the state of the semiconductor surface as a result of the applied DC gate voltage and corresponding surface potential. Overall, this charge consists of the accumulation layer charge (Q_A), depletion layer charge (Q_d), and the inversion layer charge (Q_I). With $Q_s = Q_A + Q_d + Q_I$, Eq. (2.2) becomes:

$$C = -\frac{1}{\frac{\partial V_{ox}}{\partial Q_s} + \frac{\partial \varphi_s}{\partial Q_A + \partial Q_d + \partial Q_I}} \tag{2.3}$$

Following the general definition for capacitance given by Eq. (2.1), the overall expression for the MOS capacitance can then be written as,

$$C = \frac{C_{ox}(C_a + C_d + C_i)}{C_{ox} + C_a + C_d + C_i} \tag{2.4}$$

where the oxide capacitance is determined by the oxide permittivity (ε_{ox}) and the oxide thickness (t_{ox}):

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.5}$$

Apart from the dependence on the DC gate bias, the C–V characteristics of a MOS capacitor are also dependent on the AC signal frequency and the sweep rate of the DC bias. These dependencies primarily occur in strong inversion as shown in Fig. 2.2, since a certain time is required to generate the minority carriers in the inversion layer. If the DC bias is swept slowly enough to allow the inversion layer to form and the AC measurement signal frequency is sufficiently low enough to allow the minority carriers to respond, then the device is considered to be in thermal equilibrium and a low-frequency (LF) or quasi-static curve is obtained. If the inversion layer forms but the AC signal frequency is too high for the minority carriers to respond, then a high-frequency (HF) is obtained. A deep-depletion (DD) curve is obtained when the DC sweep rate is excessive and no inversion layer can form, irrespective of the measurement frequency. Energy-band diagrams will be used in the following sections to provide a deeper insight into the principal of operation and characteristic modes of MOS capacitors.

2.2.1 Flat-band and Zero Bias Conditions

The energy-band diagram of an *ideal* MOS capacitor (no built-in charges) with a P-type substrate under flat-band conditions is illustrated Fig. 2.2a. As the condition implies, the energy bands throughout the semiconductor are flat (no band bending) and thus, the net charge at the capacitor plates, the electric field and the electric potential difference in the semiconductor

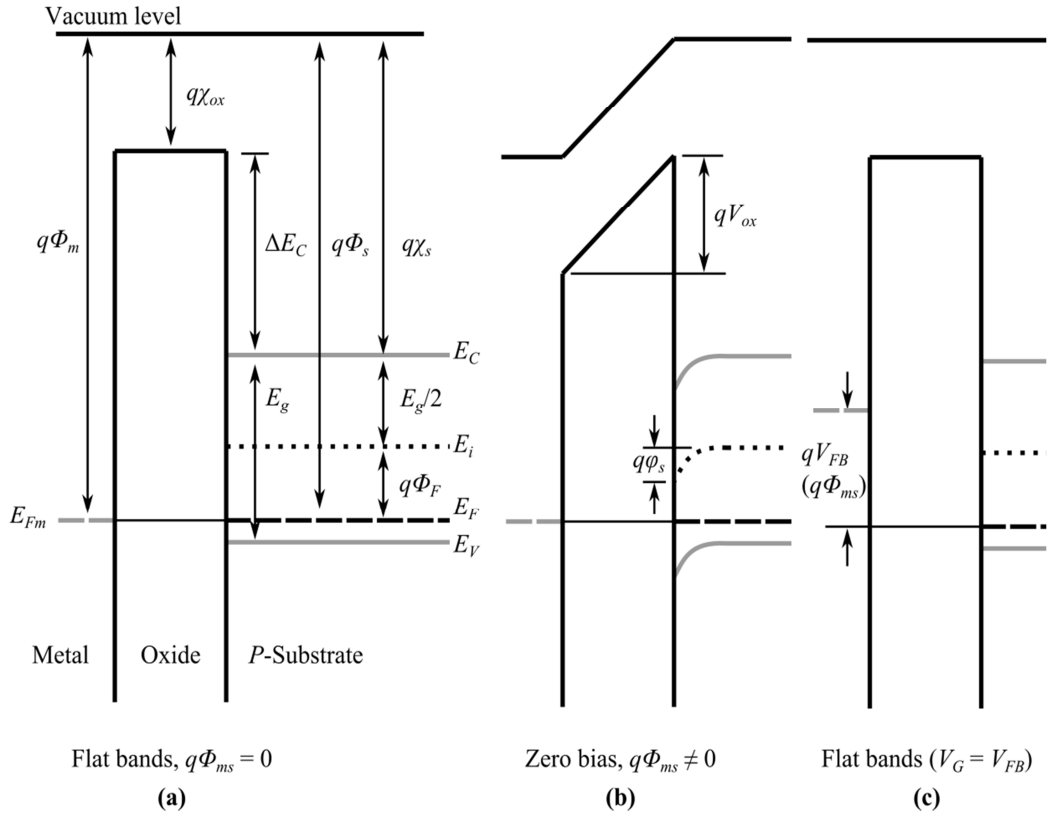

Figure 2.3 Energy-band diagrams of a MOS capacitor at zero bias and flat-band conditions. (a) A MOS capacitor with zero metal-semiconductor work-function difference and zero applied gate voltage at flat-band condition (*ideal* MOS capacitor approach). (b) Band-bending at zero applied gate voltage due to nonzero work-function difference. (c) Flat-band condition with applied gate voltage, $V_G = V_{FB} = q\phi_{ms}$.

surface region—the surface potential, are all zero. In the case of Fig. 2.3a, where the metal-semiconductor work-function difference is assumed to equal zero (the ideal MOS capacitor approach), the flat-band condition would occur at zero applied gate voltage. However, the difference that exists between the metal and semiconductor work-functions generates a built-in potential difference and a corresponding built-in electric field. As a result, the voltage across the oxide is not zero and the bands in the semiconductor

surface region are bent at V_G = 0 to account for the potential difference in the system (Fig. 2.3b). The gate voltage required to compensate for this built-in potential difference and set the surface potential to zero (the flat-band condition) is referred to as the flat-band voltage. Therefore, the flat-band condition is met when $V_G = V_{FB}$ as demonstrated in Fig. 2.3c, where the flat-band voltage simply appears as a gate-voltage offset. Consequently, the *effective* gate voltage can be expressed by $V_G - V_{FB}$.

The voltage applied between the gate and substrate is conveyed by the split between the Fermi level of the gate metal (E_{FM}) and semiconductor (E_F) in the energy-band diagrams. Because the Fermi levels are split by a potential equal to the metal-semiconductor work-function difference to attain flat bands, it can be deduced that the flat-band voltage is equal to the work-function difference ($V_{FB} = q\phi_{ms}$), if there are no additional charges present in the oxide or at the oxide-semiconductor interface.

From the energy-band diagram of Fig. 2.3a, the semiconductor work-function can be defined as

$$q\phi_s = q\chi_s + \frac{E_g}{2} + q\phi_F \tag{2.5}$$

where $q\chi_s$ is the electron affinity, $E_g/2$ is half the semiconductor energy band-gap and $q\phi_F$ is the Fermi potential. For a P-type substrate, the Fermi potential can be calculated from the following equation:

$$q\phi_F = kT \ln \frac{N_A}{n_i} \tag{2.6}$$

Using Eqs. (2.5) and (2.6), the metal-semiconductor work-function difference can be expressed as:

$$q\phi_{ms} = q\phi_m - q\phi_s = q\phi_m - \left(q\chi_s + \frac{E_g}{2} + kT\ln\frac{N_A}{n_i}\right) \tag{2.7}$$

Under flat band conditions, the MOS capacitance can be represented by a series connection of oxide and semiconductor capacitances. In this case, the semiconductor capacitance is given by $C_s = \varepsilon_s/L_D$, where ε_s is the semiconductor permittivity and L_D is referred to as the *Debye length*. The Debye length is given by

$$L_D = \sqrt{\frac{\varepsilon_s kT}{q^2 N_A}} \tag{2.8}$$

Since $C_{ox} = \varepsilon_{ox} / t_{ox}$, the *flat-band capacitance* is therefore,

$$\frac{1}{C_{FB}} = \frac{1}{C_{ox}} + \frac{1}{C_s} = \frac{t_{ox}}{\varepsilon_{ox}} + \frac{L_D}{\varepsilon_s} = \frac{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right) L_D}{\varepsilon_{ox}} \tag{2.9}$$

$$C_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)\sqrt{\frac{\varepsilon_s kT}{q^2 N_A}}} \tag{2.10}$$

2.2.2 Accumulation

A negative effective gate voltage ($V_G - V_{FB} < 0$) attracts majority carriers (holes) to the surface of the semiconductor. The accumulation of holes in semiconductor surface region signifies that the Fermi level at the semiconductor surface is closer to the valence band than in the semiconductor bulk. Therefore the energy bands are bent upward from the substrate towards the gate due to the effective applied bias ($qV_G - qV_{FB}$), as shown in Fig. 2.4. The amount of band bending in the semiconductor surface region is directly related to the value of the surface potential. Note that the convention for the surface potential is negative for upswept bands ($\varphi_s < 0$).

Using equilibrium statistics, the semiconductor surface concentration of holes (p_s) and electrons (n_s) can be expressed in terms of the surface potential as follows:

$$p_s = N_A \exp(\frac{-q\varphi_s}{kT}) \tag{2.11}$$

$$n_s = \frac{{n_i}^2}{\mathrm{p_s}} = n_{p0} \exp(\frac{q\varphi_s}{kT}) \tag{2.12}$$

where $n_{\mathrm{p0}} = {n_{\mathrm{i}}}^2/N_{\mathrm{A}}$ is the equilibrium concentration of the minority carriers (electrons) in the semiconductor bulk. Thus the density of holes at the semiconductor exponentially increases as the top of the valence band approaches the Fermi level at the surface of the substrate. Accordingly, only a slight reduction in the surface potential is required to significantly increase the density of occupied energy levels in the valence band by holes. Therefore, the change in the surface potential becomes much smaller than

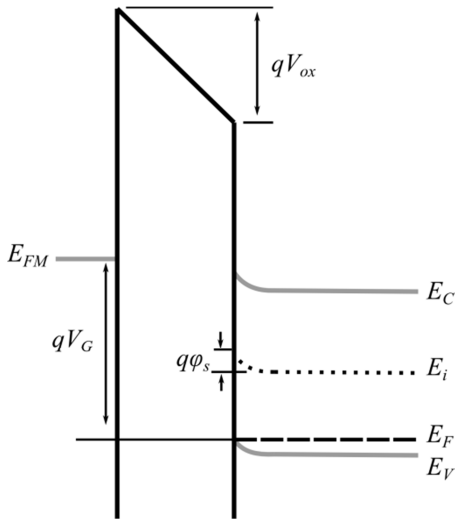

Figure 2.4 Energy-band diagram of a P-type MOS capacitor in accumulation ($\varphi_s < 0$).

the change in the effective gate voltage and almost the entire change in the gate voltage appears across the oxide (qV_{ox}).

As an incremental change in the applied gate voltage (∂V_G) results in a corresponding change in the density of accumulation charge (∂Q_A); the structure can be treated as an ordinary metal–dielectric–metal capacitor with a highly conductive sheet of holes at the substrate surface acting as the second metal plate and the gate oxide as a dielectric equivalent. The overall capacitance of a MOS structure in accumulation is, therefore, equal to the gate oxide capacitance, C_{ox}, and is independent of the gate voltage. This capacitance is used to relate Q_A to V_G:

$$Q_A = (V_G - V_{FB})C_{ox} \qquad V_G \leq V_{FB} \tag{2.13}$$

2.2.3 Depletion

Holes are depleted from the semiconductor surface, forming a depletion layer when a relatively small positive effective voltage is applied to the gate ($V_G - V_{FB} > 0$). The small gate voltage increase above the flat-band value causes energy bands to bend downward, increasing the potential difference between the top of the valence band and the Fermi level at the surface of the substrate, as illustrated in Fig. 2.5. In depletion, the net charge that appears at the surface region of the substrate is due to negative acceptor ions in the depletion layer. The depletion layer charge density (Q_d) that compensates for the increasing voltage at the gate is modulated by altering the depletion layer width:

$$Q_d = qN_A w_d \tag{2.14}$$

where the width of the depletion layer can be related to the surface potential by

$$w_d = \sqrt{\frac{2\varepsilon_s \varphi_s}{qN_A}} \tag{2.15}$$

The MOS capacitance in depletion can be represented by a series connection of the oxide and depletion layer capacitances. In this case, the depletion layer capacitance is given by $C_d = \varepsilon_s/w_d$. Therefore, the total MOS capacitance is

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_d} = \frac{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right) w_d}{\varepsilon_{ox}} \tag{2.16}$$

$$C = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)\sqrt{\frac{2\varepsilon_s \varphi_s}{qN_A}}} \tag{2.17}$$

Equation (2.17) shows that the MOS capacitance is reduced as w_d increases, where the minimum capacitance is obtained when the depletion layer is at maximum width. This capacitance versus voltage dependence of MOS capacitors in the depletion regime has been found to be extremely useful in the evaluation of the electrical properties of oxide-silicon interfaces.

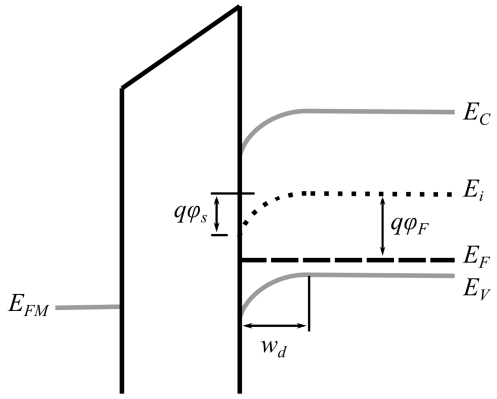

Figure 2.4 Energy-band diagram of a P-type MOS capacitor in depletion ($0 < \varphi_s < 2\varphi_F$).

However, Eq. (2.15) gives the depletion layer width in terms of the surface potential and not in terms of the applied gate voltage. Therefore, a linking equation is required to relate the surface potential and the gate voltage to determine w_d and subsequently, calculate the C–V dependence given by Eq. (2.17). This correlation between the effective gate voltage and the surface potential can be expressed in the following form [5]:

$$V_G - V_{FB} = \varphi_s + \gamma\sqrt{\varphi_s} \tag{2.18}$$

where $0 < \varphi_s \leq 2\phi_F$ and

$$\gamma = \sqrt{\frac{2\varepsilon_s q N_A}{C_{ox}}} \tag{2.19}$$

is referred to as the *body factor,* which incorporates all the technological parameters.

2.2.4 Strong Inversion

By further increasing the applied gate voltage, the energy band-bending will bring the bottom of the conduction band closer to the Fermi level and $E_C - E_F$ will become smaller than $E_F - E_V$. Surface carrier statistics show that the concentration of thermally generated minority carriers (electrons) will then surpass the majority carrier (hole) concentration Therefore, the surface of the semiconductor is said to be *inverted*. As the MOS capacitor enters the inversion region, the surface potential begins to become less dependent of the applied gate voltage because the induced gate oxide field is screened by an increasing density of electrons in the inversion layer. When the screening becomes so efficient that the surface potential becomes effectively *pinned*, the MOS capacitor is said to be in *strong inversion*. This mode of operation is of particular importance because the high concentration of

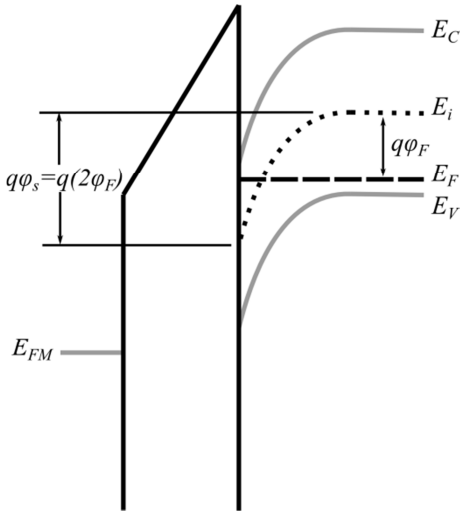

Figure 2.6 Energy-band diagram of a P-type MOS capacitor in strong inversion ($\varphi_s \geq 2\phi_F$).

electrons in the inversion layer at the surface of the substrate creates the highly conductive channel in enhancement mode MOSFETs.

The energy-band diagram of a P-type MOS capacitor in strong inversion is illustrated in Fig. 2.6. The value of the surface potential at the onset of strong inversion is defined as

$$\varphi_s = 2\phi_F \tag{2.20}$$

where ϕ_F is the Fermi potential, which is defined by Eq. (2.6). The gate voltage that corresponds to the onset of strong inversion is called the *threshold voltage* (V_T). By applying the threshold condition, $V_G = V_T$ when $\varphi_s = 2\phi_F$, to Eq. (2.18) the threshold voltage can be calculated from the following expression:

$$V_T = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \qquad (2.21)$$

In this described mode of strong inversion, any change in the gate oxide field induced by a change in the applied gate voltage beyond the threshold voltage is perfectly screened by a corresponding change of the electron concentration in the inversion layer. Consequently, the structure can be treated as an ordinary metal–dielectric–metal capacitor with a highly conductive sheet of electrons at the substrate surface acting as the second metal plate and the gate oxide as a dielectric equivalent. The MOS capacitance in strong inversion is, therefore, equal to the gate oxide capacitance, C_{ox}, and is independent of the gate voltage. Accordingly, the inversion-layer charge is modeled by

$$Q_I = (V_G - V_T)C_{ox} \qquad (V_G \geq V_T) \qquad (2.22)$$

The described behaviour of a MOS capacitor in strong inversion is only valid under the condition that there is a sufficient supply of electrons to respond to the changes in the gate oxide field. In a MOSFET, an abundance of electrons is supplied by the source contact, whereas, the supply of electrons in the case of a MOS capacitor is limited to thermal generation. The thermal generation of minority carriers is a relative slow process, and is not able to respond to fast oscillations of the AC measurement signal. Therefore, the described behaviour of a MOS capacitor that coincides with the operation of a MOSFET in strong inversion is according to the low-frequency (or quasistatic) model illustrated in Fig. 2.2, where $C_{LF} = C_{ox}$. If the signal oscillations are faster than the thermal generation time then the inversion layer charge will not be able to respond to the oscillations in the oxide field and the increasing gate charge will be balanced by the depletion layer charge. The MOS capacitance measured

under high-frequency (C_{HF}) conditions will therefore be modelled by the series capacitance of C_{ox} and C_d. This model is the same as used in the depletion region [Eqs. (2.16) and (2.17)] however the surface potential is approximately pinned at the strong inversion value of $2\phi_F$. As a result, the capacitance in strong inversion remains at its minimum value that corresponds to the maximum depletion layer width:

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_d} = \frac{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right) w_{d(\max)}}{\varepsilon_{ox}} \tag{2.23}$$

$$C_{HF} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_s}\right)\sqrt{\frac{4\varepsilon_s \phi_F}{qN_A}}} \tag{2.24}$$

The MOS capacitance in strong inversion at high-frequency is shown in Fig. 2.2. This behaviour however, will only be observed if the inversion layer is fully created when the high-frequency measurement is performed. If the sweep rate of the DC gate bias is much greater than the thermal generation rate of electrons then no inversion layer will be formed, and the value of the MOS capacitance at biases corresponding to the strong inversion region will continue to decrease from the depletion region into what is referred to as *deep depletion (*the curve labelled DD in Fig. 2.2*)*. The deep depletion C–V behaviour is almost always observed at room-temperature for MOS capacitors fabricated on wide band-gap materials, such as silicon carbide, because the thermal generation rate of electrons is much slower (virtually inhibited) than any practical sweep rate of applied gate bias.

2.3 ELECTRICAL CHARACTERISATION: NON-IDEAL EFFECTS IN MOS CAPACITORS

In practice, the experimentally measured behaviour of a MOS capacitor will always deviate from the theoretical case to a specific degree. This is caused

by additional sources of charge stemming from electrically unpassivated dangling bonds and other atomic scale defects that are formed at or in close proximity to the semiconductor–oxide interface during the thermal oxidation process. As a result, the underlying semiconductor will induce additional charge of opposing polarity to maintain charge neutrality, $Q_G = -(Q_s \pm Q_{eff})$, where Q_{eff} denotes the overall effective charge resulting from the defect centers, which can either be positive or negative in nature. Accordingly, it becomes apparent that the flat-band and threshold voltages of MOS devices can strongly be affected by these charges.

The amount of additional charge induced in the semiconductor will be inversely proportional to the distance the charge is located from the surface of the semiconductor [4]. Therefore, a defect center residing very near the semiconductor surface will reflect all of its charge in the semiconductor, whereas a center located near the metal–oxide interface will cause little or no effect in the semiconductor. Due to the discontinuation of the crystal lattice periodicity at the semiconductor surface, the oxide-semiconductor interface that is formed during thermal oxidation is not abrupt but separated by a narrow transitional region which extends from the semiconductor surface to the amorphous oxide layer [7]. Residing within this transitional region are two sources of additional charge. According to standardised nomenclature they are referred to as *fixed oxide charge* and *interface trapped charge* [8]. Their densities are strongly related to oxidation processing conditions such as the oxidation ambient and temperature and therefore should be controlled or minimized during the fabrication process. The most popular methods to quantitatively measure these charges as described in the in the texts by Nicollian and Brews [4], Schroder [6] and Sze [7] will be reviewed in the following sections.

2.3.1 Measuring Fixed Oxide Charge

Fixed oxide charge (Q_f) is generally positive in nature and is located a few nanometres away from the surface of the substrate, in the transitional region. At this distance, the charge is not in electrical communication with the underlying substrate and is therefore unaffected by variations in the applied gate voltage. It acts as a *fixed* voltage offset and shifts the entire C–V curve, analogous to that of the built-in charge associated with the metal–semiconductor work-function difference. The fixed oxide charge can be determined by comparing the flat-band voltages of the experimentally measured and theoretically calculated C–V curves, as shown in Fig.2.7. In order to determine the flat-band voltage shift between the two curves, the flat-band capacitance must firstly be determined. Provided the doping density and gate oxide thick are know, the flat-band capacitance can be calculated from Eqs. (2.8), (2.9) and (2.10). The oxide charge can then be related to the flat-band voltage by the equation [6],

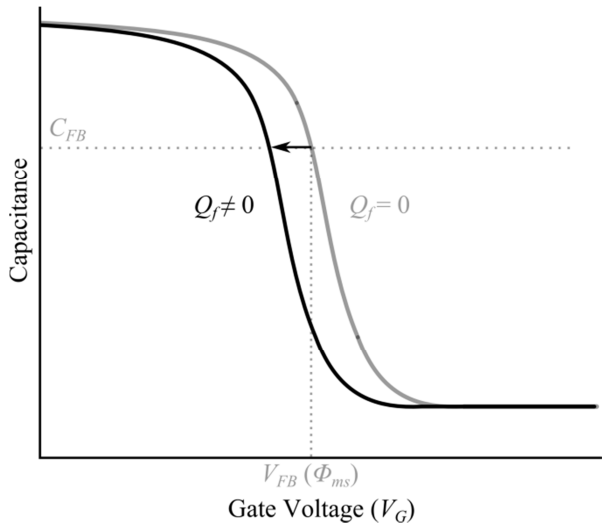

Figure 2.7 The effects of fixed oxide charge on the C–V characteristics of an ideal ($Q_f = 0$) P-type MOS capacitor.

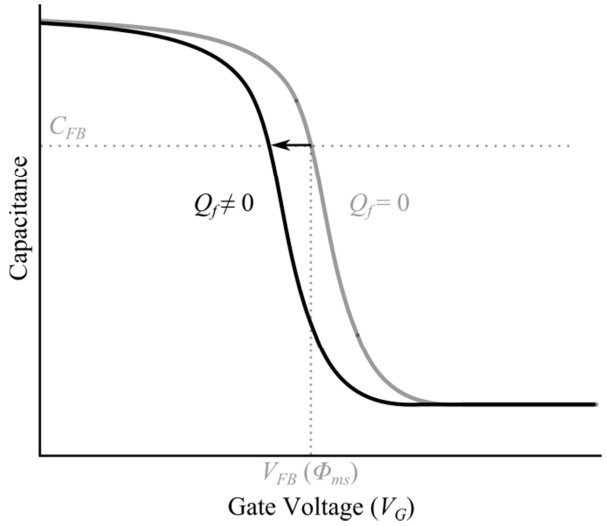

Figure 2.7 The effects of fixed oxide charge on the C–V characteristics of an ideal ($Q_f = 0$) P-type MOS capacitor.

$$Q_f = (\phi_{ms} - V_{FB})C_{ox} \tag{2.25}$$

thus the theoretical curve ($V_{FB} = V_{FB} - \phi_{ms}$) will simply be shifted by the amount, Q_f/C_{ox}. This equation assumes that the experimentally measured curve is free of any other charges. In reality, the measured curve will also contain contributions from mobile ionic charge (Q_m), oxide trapped charge (Q_{ot}) and interface trapped charge (Q_{it}) [4]. Simple measurements of the fixed oxide charge using C-V measurements generally cannot distinguish between the individual charges therefore Q_f becomes the *effective oxide charge*, (Q_{eff}).

2.3.2 Measuring the Interface Trap Density

Historically, interface traps in the Si/SiO_2 system are considered to be spatially located at the semiconductor-oxide interface where they can readily exchange charge with majority carriers from either the bottom of the

conduction band or the top of the valance band of the underlying substrate [8]. Conversely, in more recent times it has been suggested that near-interface oxide traps or border traps that reside in the narrow transitional region in close proximity to the semiconductor surface can also exchange charge with the underlying substrate and thus, also act as interface traps [9]. However, it is usually unclear as to whether non-ideal MOS device characteristics are caused by interface or near–interface traps due to their very similar electrical behaviour and both are still regularly grouped together and simply referred to as "*interface traps*" [9]. Energetically, these traps are situated so close together that they form a continuum of energy levels residing within the semiconductor bandgap [10-12]. Since the interface trap energy levels are dispersed across the bandgap, their density (D_{it}) is defined as [7]

$$D_{it} = \frac{1}{q}\frac{\partial Q_{it}}{\partial E} \quad \text{charges/cm}^2\text{eV} \tag{2.26}$$

` where Q_{it} represents the associated interface trapped charge.

In thermal equilibrium the electron occupancy of an interface trap, located at energy level (E_T) is given by a Fermi-Dirac distribution function [4]:

$$f = \frac{1}{1 + g\ exp\left(\frac{E_T - E_F}{kT}\right)} \tag{2.27}$$

where k is the Boltzmann's constant, T is the absolute temperature and E_F is the Fermi-level at the semiconductor surface.

The ground-state degeneracy factor (g) is determined by the behaviour of the trap, with g = 2 for donors and g = 4 for acceptors [7]. In the Si/SiO_2 system, donor-like traps are generally considered to be

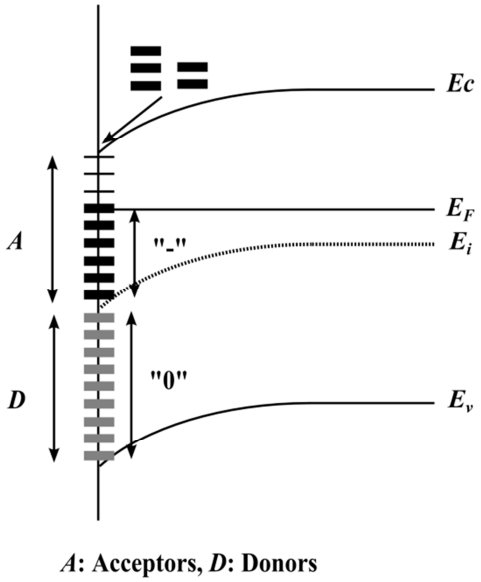

Figure 2.8 Energy band diagram of an N-type Si MOS capacitor in accumulation, illustrating the interface trap occupancy and trap behaviour. All traps below the Fermi-level are essentially occupied by electrons from the conduction band as indicated by the short thick lines. Unoccupied traps are indicated by the thin lines. In this case the trapped charge is either neutral (0) or negative (–) depending on the trap behaviour and occupancy.

energetically located in the lower-half of the bandgap, where they are positively charged when empty and electrically neutral when occupied. In contrast, acceptor-like trap states are energetically located in the upper-half of the bandgap, where they are electrically neutral when un-occupied and negatively charged when they are occupied. This behaviour is illustrated in Fig. 2.8 for an N-type MOS capacitor, where the majority carriers are electrons.

The gate bias induced surface potential determines the trap energy position (E_T) at the surface of the semiconductor with respect to the bias invariant Fermi-level in the semiconductor bulk, and, consequently, the occupancy of the trap. A trap state will become electrically active and

dynamically capture and emit of a free carriers from the underlying semiconductor if it is approximately energetically aligned to the Fermi energy. The Fermi-Dirac distribution function of Eq. (2.27) implies that the probability of occupancy is essentially unity if it is situated a few kT below E_F. Once the trap is occupied no further transfer of electrons are permissible to and from that state as it is essentially charged. On the other hand, if trap is situated a few kT above E_F, the probability of occupancy is essentially zero and no electron-trap transition will occur due to the unfavourable energetic transition for electrical excitation to occur.

The capture and emission of majority carriers to and from the majority band by the electrically active interface trap is not instantaneous but occur over a finite time. The response time trap response time (τ_{it}) is governed by classical Shockley-Read-Hall (SRH) statistics. For N-type substrates, the trap response time between conduction band electrons and interface traps can be defined by the emission rate (τ_e) as [13]:

$$\tau_{it} \approx \tau_e = \frac{\exp\left[\frac{(E_C - E_T)}{kT}\right]}{\sigma \vartheta_{\mathrm{th}} \mathrm{N_C}} \tag{2.28}$$

where E_c is the energy level of the conduction-band minima, σ the trap capture cross section, ϑ_{th} the thermal velocity of electrons and N_C is the effective density of states in the conduction-band. Equation (2.28) implies that the trap response time is exponentially dependent on the energetic trap position with respect to the conduction–band and is also temperature dependent.

The Measured MOS Impedance: Influence of Interface Traps

Impedance measurements based on the small-signal response of the MOS capacitor as a function of gate bias, frequency and temperature include contributions from the interface trapped charge, as well as other valuable information such as the oxide thickness, surface potential and substrate

doping concentration. These measurements are generally made by applying a DC bias that is swept in staircase fashion superimposed with a small amplitude AC signal at a fixed frequency to the metal gate of a MOS capacitor.

The AC signal causes periodic fluctuations of the surface potential causing the trap energy level to oscillate in the proximity of the Fermi-level, with respect to the energy level position as determined by the DC gate bias. Provided the characteristic trap response time is comparable to, or quicker than the period of the measurement frequency the traps will be able to follow the ac signal and will contribute both an equivalent parallel capacitance (C_P) and an equivalent parallel conductance (G_P) to the basic

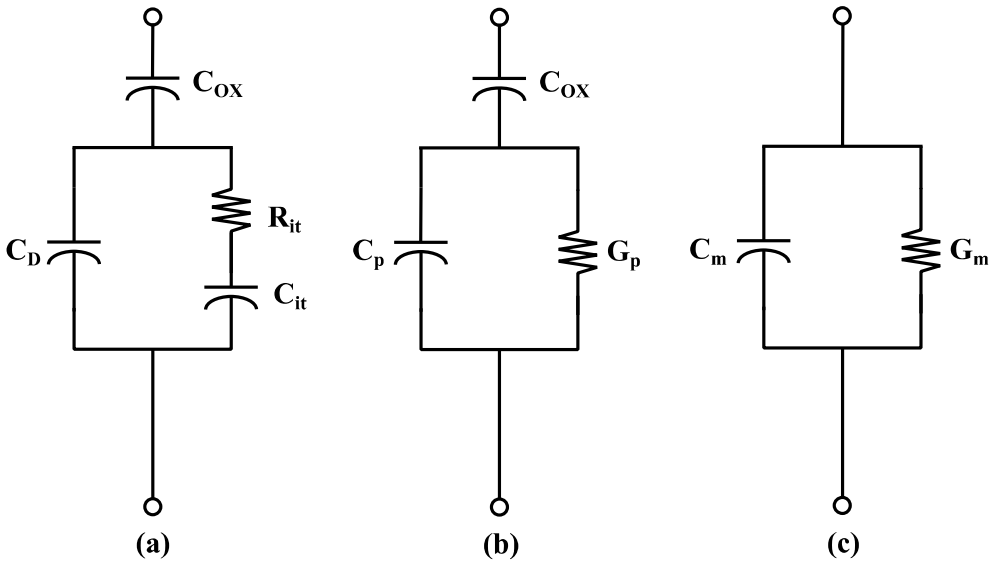

Figure 2.9 Equivalent circuits of a MOS capacitor in depletion containing interface traps: (a) including interface state loss product of C_{it} and R_{it}, (b) simplified circuit of (a) containing the equivalent parallel capacitance Cp and conductance G_p and (c) the equivalent circuit of the measured capacitance C_m and measured conductance G_m obtained by a semiconductor parameter analyser or LCR bridge.

equivalent circuits of a MOS capacitor as shown in Fig. 2.9 [6]. This model is strictly based on the MOS capacitor in depletion, where the depletion capacitance is paralleled with the frequency and surface potential dependent interface trap capacitance (C_{it}) associated with the interface trapped charge.

The loss associated with the SRH transitions is represented by the interface trap resistance (R_{it}). The series product of the interface trap resistance and capacitance represents the trap response time which determines the frequency behaviour. From the basic equivalent circuits shown in Fig. 2.9, the parallel capacitance and conductance can be defined by

$$C_P = C_d + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \tag{2.29}$$

and

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau}{1 + (\omega\tau_{it})^2} \tag{2.30}$$

where ω is the angular frequency, and

$$\tau_{IT} \equiv C_{it}R_{it} \tag{2.31}$$

LCR bridges and semiconductor parameter analyzers commonly represent the MOS capacitor as a parallel, measured capacitance (C_m) – conductance (G_m) combination as shown in Figure 2.4c. From Figure 2.4b, C_p and G_p can be obtained in terms of the measured capacitance and the measured conductance by the following equations [14]:

$$G_P = \frac{\omega^2 G_m {C_{ox}}^2}{{G_m}^2 + \omega^2 (C_{ox} - C_m)^2} \tag{2.32}$$

and

$$C_P = \frac{C_{ox}\left[{G_m}^2 + \omega^2 C_d (C_d + C_{ox})\right]}{\omega^2 (C_d + C_{ox})^2 + G_m} \tag{2.33}$$

As long as the interface trap density (D_{it}) does not significantly fluctuate with the trap energy level position then it can be related to the interface trap capacitance by [4]

$$D_{it} = \frac{C_{it}}{q} \tag{2.34}$$

Since equations (2.29) and (2.40) both contain the same interface trap contributions, either capacitance-voltage (C–V) or conductance-voltage

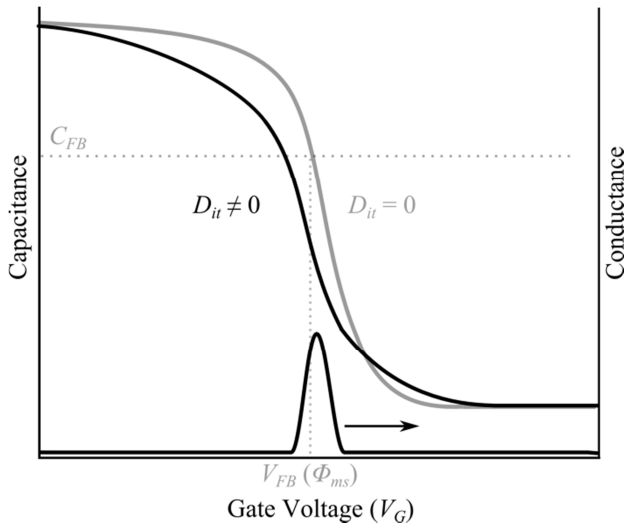

Figure 2.10 The effects of interface traps on the C–V and G–V characteristics of a P-type MOS capacitor. The interface trap density is denoted by $D_{it.}$

(G–V) measurements can be used to obtain D_{it}, as inferred by Eq. (2.34). Methods based on the measured C–V admittance response of a MOS capacitor are generally the simplest and quickest means to obtain the interface trap density as a function of energy level. Information on interface trap density using capacitance based measurements is obtained by analysing the *stretch-out* between theoretical and measured curves. The stretch-out is due to the change in interface trap occupancy and associated interface trapped charge. As the interface traps are distributed at energy levels within the band-gap, the experimentally measured C–V curve will exhibit distortion unlike the parallel shift associated with fixed oxide charge [4, 6, 7]. If the traps are in resonance or partial resonance to the AC small signal then the C–V stretch-out will be complimented by an AC conductance component [4]. These effects are illustrated in Fig. 2.10. The most popular methods to estimate the D_{it} using C–V and G–V measurements will be reviewed in the subsequent sections.

High-frequency C–V (Terman) Method

The high frequency capacitance method, pioneered by Terman [12], is one of the earliest techniques for determining the interface trap density. In this method the MOS capacitance is measured as a function of gate bias at a frequency sufficiently high enough that the interface traps do not respond to the superimposed, AC small signal. Since the interface traps do not respond to the measurement frequency the equivalent circuit of the MOS capacitor in depletion at high frequencies, is simply the series combination of the oxide and depletion layer capacitances given by the following equation:

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_d} \tag{2.35}$$

The high frequency response is therefore comparable to that of an ideal MOS capacitor, free of interface traps, provided that the semiconductor

capacitance as a function of the surface potential is identical in both cases. However, although the traps do not respond to the high frequency signal they do respond to the slowly varying gate bias when MOS capacitor is swept between accumulation and inversion regions. This is due to the charging of the interface traps as they change occupancy and consequently induce additional trap charge (Q_{it}), which causes the high-frequency curve to stretch-out along the gate voltage axis. As a result a non-parallel shift is typically observed due to the distribution of the interface traps in comparison to a theoretical curve [4].

To maintain charge neutrality, a larger gate bias is required owing to the effect additional trapped charge on the surface potential. For this reason, the measured high-frequency C–V curve can be expressed using Guass's law by modifying Eqn (2.2) to include the interface trapped charge, Q_{it} [4]:

$$C_{ox}(V_g - \phi_s) = -[Q_{it}(\phi_s) + Q_d(\phi_s)] \tag{2.36}$$

By substituting

$$C_{it}(\phi_s) \equiv -\frac{dQ_{it}}{d\phi_s} \tag{2.37}$$

and

$$C_d(\phi_s) \equiv -\frac{dQ_d}{d\phi_s} \tag{2.38}$$

into Eq. (2.36), the relationship between a slight change in gate bias (∂V_G) and a slight change in the surface potential ($\partial\phi_s$) can be expressed by:

$$C_{ox}\,\partial V_G = [C_{ox} + C_{it}(\phi_s) + C_d(\phi_s)]\partial\phi_s \tag{2.39}$$

All the relevant trap information can therefore be extracted from the surface potential and gate bias relationship between the experimental ($Q_{it} \neq o$) and a theoretical C–V curve ($Q_{it} = o$) free of interface traps.

The semiconductor capacitance is a known function of the surface potential for a given doping concentration and can be used to obtain the relationship between ϕ_s and V_G [6]. The influence of the interface trapped charge can therefore be examined from the stretch-out between the measured and theoretical *C–V* curves by:

$$C_{it}(\phi_S) = C_{ox}\left(\frac{\partial V_G}{\partial \phi_S} - 1\right) - C_d(\phi_S) \tag{2.40}$$

and the interface trap density can be inferred using Eq. (2.34),

$$D_{it}(\phi_s) = \frac{C_{ox}}{q}\left(\frac{\partial V_G}{\partial \phi_S} - 1\right) - \frac{C_d(\phi_s)}{q} \tag{2.41}$$

where the oxide capacitance can simply be measured in strong accumulation.

While the estimation of the interface trap density using the high frequency method is simple and can be rapidly obtained, it relies on the accuracy of calculating the theoretical ideal capacitance curve as a function of the surface potential. To obtain the theoretical curve the semiconductor the doping profile and the oxide thickness must be known. The doping profile is generally assumed to be uniform however this is seldom the case [15]. Inaccuracies in determining these parameters can introduce ambiguity into theoretical curve thereby providing a significant source of error in estimating the interface trap density.

Quasi-static C–V Method

The interface trap density can also be extracted from the experimental low-frequency C–V measurements. This technique assumes that the measurement frequency is so low that all the interface traps can maintain equilibrium with the applied AC signal at any instant of time [16]. Because of the difficulties involved with capacitance measurements at low-frequencies (*1 - 10 Hz*), a *quasistatic* low-frequency approach is generally preferred. A quasistatic C–V curve is obtained by applying a slow, linearly ramped gate bias (constant $\partial V/\partial t$) and measuring the resulting displacement current (I_{QS}) which is directly proportional to the incremental low frequency MOS capacitance (C_{LF}) [17]:

$$I_{QS}(V) = C_{LF}(V)\,\partial V/\partial t \tag{2.42}$$

Because it is assumed that all the traps can respond to the slowly ramped gate bias they will contribute an additional trap capacitance (C_{it}) to the measured C–V characteristic in depletion. Furthermore, since the traps will respond to the slowly changing gate bias they will also induce stretch-out to the C–V curve along the gate bias axis in similar fashion to high-frequency measurements. The overall MOS capacitance is depletion under quasistatic of low-frequency conditions can therefore be expressed as

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_d + C_{it}} \tag{2.43}$$

Solving for C_{it} yields ,

$$C_{it} = \left(\frac{1}{C_{ox}} - \frac{1}{C_{LF}}\right)^{-1} - C_d \tag{2.44}$$

and the interface trap density can be obtained by:

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}\,C_{LF}}{C_{ox} - C_{LF}} - C_s\right) \tag{2.45}$$

Analogous to the high frequency technique, the theoretical calculation of semiconductor capacitance as a function of the surface potential is required to extract the interface trap density. However, in this method the surface potential can be determined within an additive constant. This can be obtained directly from the measured C–V curve when in thermal equilibrium by the Berglund integral [16]:

$$\phi_S(V_G) = \phi_{s0} + \int_{V_{G0}}^{V_G}\left[1 - \frac{C_{LF}\,(V_G)}{C_{ox}}\right]dV_G \tag{2.45}$$

To minimize the uncertainty of the additive constant (ϕ_{s0}) the initial gate bias (V_{G0}) should be chosen in accumulation or inversion where the band banding becomes a weak function of the gate bias.

This method avoids the errors associated with the determination of the ϕ_s verses V_G curve in the high-frequency method however; uncertainty in the additive constant can still provide a source of error. The low-frequency method still requires the theoretical calculation of C_s to extract the D_{it} and therefore still suffers from similar inaccuracies as the high-frequency method due to erroneous determination of the substrate doping profile.

High-low Frequency C–V Method

The shortcomings involved with the difficulties of accurately determining the doping profile and calculating a theoretical C–V curve in the previously discussed methods can be alleviated by implementing the high-low frequency method developed by Castagné and Vapaille [18]. This method extracts the D_{it} from the differential capacitance between simultaneously measured high- and low-frequency C–V curves. In doing so

this method eliminates the uncertainty associated with the calculation of C_d in Eq. (2.44) with a experimentally measured C_d. Rearranging Eq. (2.35) from the high-frequency curve for C_d yields,

$$C_s = \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \tag{2.46}$$

allows the low-frequency expression for C_{it} of Eq. (2.44) to be rewritten in the form:

$$C_{it} = \left(\frac{1}{C_{ox}} - \frac{1}{C_{LF}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \tag{2.47}$$

where C_{it} is related to D_{it} by Eq. (2.34) which gives D_{it} in terms of the measured high and low frequency *C–V* curves as

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{ox}C_{HF}}{C_{ox} - C_{HF}}\right) \tag{2.48}$$

The interface trap density as a function of surface potential can be simply obtained by using the low-frequency curve to determine the ϕ_s verses V_G relationship using the Berglund integral.

The high-low capacitance method is a simplified approach to determine the interface trap density in comparison the previously described techniques as it does not require the computation of a theoretical C–V curve. This is also advantageous as it eliminates the errors introduced through the ambiguity of determining the doping profile as previously mentioned. While the high-low capacitance method removes the uncertainties associated with the theoretical curve it is still limited in applicability and accuracy due to the fundamental issues inherent to all *C–V* based methods.

The basic prerequisite common to all *C–V* based methods is that the measured *C–V* curves are indeed true representations of high and low frequency curves. To satisfy this requirement it is considered that all traps should be able to respond to the low frequency measurement whereas no traps should be able to respond to the high frequency measurement conditions; otherwise the inferred D_{it} will be erroneous. Accordingly, the *C–V* measurements can only be truly represented over a limited portion of the bandgap by applying practical measurement frequencies. Since the trap response time is dependent on the trap energy level, with respect to the majority band edge, the traps bordering the majority band edge will respond almost instantaneously, whereas the response time for traps situated near the minority band edge will be extremely long. Therefore realistic C–V measurements are restricted to surface potentials corresponding to the depletion or weak-inversion regions where practical response times can be obtained [4].

However, there is no way to determine the energy window in which representative data is valid directly from the measurements, as the D_{it} is graphically revealed by the difference between two C–V curves. Calculation rounding errors are also introduced due to the fact that all *C–V* techniques depend on the differential capacitance between curves to obtain C_{it}. These inaccuracies become particularly evident when the value of C_d is large in comparison to C_{it}. Overall, the *C–V* based methods require minimal measurement and computational efforts. Therefore the D_{it} distribution can be assessed quite swiftly. However caution is required to avoid misinterpretation of the results due to inaccuracies that can be manifested in both the measurement and calculation procedures. In general, *C–V* based can only yield the gross features of the oxide-semiconductor interfacial region since the measurements merely occur over one or two frequencies, thus the frequency behaviour of the traps is subsequently lost. A more

detailed summary of the limitations associated with the C–V based methods can be found in Refs. [4, 19].

AC Conductance Method

The conductance method is regarded as one of the most accurate, reliable and sensitive techniques to evaluate the properties of the MOS interface. This method was initially developed by Nicollian and Goetzberger [10, 20], based on the parallel conductance expressions derived by Lehovec [11, 21]. The conductance method not only determines interface trap density in the depletion region but also examines the full frequency dispersion of the MOS capacitance rather than just the high- and low-frequency aspects. It also permits the measurement of capture cross sections as well providing information about surface potential fluctuations [22].

While both capacitance and conductance measurements contain the same interface trap information, the conductance yields the greatest accuracy as it does not require the determination the doping density to calculate C_s nor complications associated with extracting C_{it} from the total measured capacitance that additionally contains the contributions of both the oxide and semiconductor capacitances. The equivalent parallel conductance G_p, only depends on the lossy $R_{it}C_{it}$ product from interface trap branch as shown in simplified equivalent circuit of Fig. 2.9a. This solely arises from the steady-state energy loss mechanisms associated with the capture and emission process of majority carriers in or near resonance with the time period of the measurement signal frequency. The conductance method can therefore provide a direct measure of the interface trap properties.

The conductance is generally measured as a function of frequency for various fixed values of gate bias voltage and is plotted as G_p/ω versus ω. This typically forms a symmetrical characteristic Gaussian or "*bell curve*" shaped

plot. For a given gate bias, interface traps can immediately change occupancy in phase with the ac signal at low values of $\omega\tau_{it}$ ($\omega\tau_{it} \rightarrow 0$). Therefore, no energy loss occurs and $G_p/\omega = 0$. As $\omega\tau_{it}$ increases the interface traps can no longer change occupancy immediately in response to the AC signal. They begin to lag behind due to the losses associated with the SRH transition processes [13] and consequently, give rise to measurable conductance. At high values of $\omega\tau_{it}$ traps can no longer respond to the AC signal and hardly change occupancy. Therefore energy losses no longer transpire and G_p/ω becomes negligible. The maximum energy loss occurs when the interface traps are in resonance with the measurement frequency [20]. From Eq. (2.30) this maximum will occur when $\omega\tau_{it} = 1$, thus providing τ_{it} directly. The value of G_p/ω at this maximum is $C_{it}/2$ and therefore *T*he interface trap density is directly proportional to the maximum G_P/ω and τ_{it} can be determined from the conductance peak location on the ω axis [4, 20].

This simplified equation for the parallel conductance only assumes a single trap energy level in the bandgap; however interface traps are continuously distributed throughout the bandgap, forming an energy level continuum [12]. Therefore the capture and emission process does not only occur for interface trap energy levels directly aligned to the Fermi-level at the semiconductor but are dispersed over a range of energy levels located within a few kT/q of the Fermi-level. Each interface trap level contributes a different energy loss that is dependent on the energy difference between the trap level and E_F. As a result, each trap energy level has a different time constant and therefore disperses time constant. This time constant dispersion factor is applied to the expression for the normalized conductance as follows [20, 23]:

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \qquad (2.49)$$

From Eq. (2.49) the maximum G_P/ω is found when $\omega \approx 2/\tau_{it}$. The interface trap density can therefore be estimated from the normalized parallel conductance peak by

$$D_{it} \approx \frac{2.5}{Aq}\left(\frac{G_P}{\omega}\right)_{max} \tag{2.50}$$

However, it was experimentally found that Eq. (2.50) does not fit the experimental G_p/ω vs ω curves and the observed time constant dispersion was far broader than predicted [10]. Nicollian and Goetzberger attributed this to the random distribution of built in charges and charged interface traps in the plane of the interface, giving rise to fluctuations in the electric field, causing corresponding fluctuations in the surface potential and therefore fluctuations in the trap energy level with respect to the Fermi-level. Equation (2.28) demonstrates that small fluctuations in the surface potential and the corresponding trap energy level will manifest into large fluctuations in the characteristic trap response time, therefore broadening the dispersion of the time constant. When such fluctuations are taken into account Eq. (2.49) becomes

$$\frac{G_P}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] P(U_s) dU_s \tag{2.51}$$

where $P(U_s)$ is the probability distribution function which determines the surface potential fluctuations for the continuum of interface trap levels located in a characteristic area and is given by

$$P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}} exp\left[-\frac{(\varphi_s - \bar{\varphi}_s)^2}{2\sigma^2}\right] \tag{2.52}$$

The terms $(\varphi_s - \bar{\varphi}_s)^2$ and σ^2 represent the normalized mean surface potential per characteristic area and the standard deviation respectively.

In order to assign the D_{it} to a bandgap energy level the surface potential-gate voltage relationship has to be determined. This can be calculated by measuring a low-frequency C-V curve and applying the Berglund integral as previously described. Alternatively, the characteristic trap energy level can be determined by applying Eq. (2.28) at a given frequency and corresponding gate bias where the G_p/ω curve peaks.

Unlike C–V techniques, it is virtually impossible to extract interface trap information from invalid regions of the energy bandgap due to the direct measure of their properties from the position of the G_p/ω peak. In addition, the characteristic trap response time can be determined directly and therefore information regarding the trap capture cross section can be easily obtained by evaluating Eq. (2.28). Furthermore the conductance method examines the full frequency dispersion of the MOS capacitance and therefore the full frequency behaviour of the traps can be assessed. The only major drawback of the conductance technique is that it requires extensive and elaborate acquisition of capacitance and conductance verses frequency data. This leads to significant analysis time in comparison to C–V based techniques. As an alternative to the overwhelming data acquisition using the complete conductance analysis technique an approximation method can be employed such as the method described by Hill and Coleman [24].

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3

THE ACTIVE NEAR INTERFACE TRAPS IN 4H–SiC METAL–OXIDE–SEMICONDUCTOR FIELD-EFFECT TRANSISTORS

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3.1 INTRODUCTION

The ability to correctly evaluate the SiC–SiO_2 interface in terms of the electrically active defects that dominate the channel-carrier mobility in SiC MOSFETs is crucial for the further development of passivation processes that are required to improve the electrical characteristics of these devices. This chapter begins with a critical overview on the current understanding of interface traps in SiC MOS structures and particularly, their impact on the electron transport in N-channel 4H–SiC MOSFETs. The review exposes several inconsistencies that exist from the direct application of conventional interface characterisation techniques based on Shockley-Read-Hall statistics to the SiC–SiO_2 system. One of which is the fact that conventional techniques, based on capacitance–voltage and conductance–voltage measurements of MOS capacitors, are limited to resolving electrically active defects with energy levels that correspond to gate biases in the depletion region of operation. In the case of 4H–SiC devices, the energy levels of these defects are found to be inconsistent with the factors that degrade the channel-carrier mobility in 4H–SiC MOSFETs. Based on the understanding that the Fermi level in a MOSFET inversion channel is aligned to the conduction band, due to the quantum confinement of the channel electrons, the near-interface oxide traps (NITs) energetically aligned to the 4H–SiC conduction band are considered to be directly responsible for the severe channel-carrier mobility degradation in 4H–SiC MOSFETs. An experimental demonstration reveals that these NITs can be detected by AC conductance measurements of MOS capacitors in accumulation. It is also demonstrated that the transfer mechanism between the channel-carriers and the active NITs is due to thermally independent tunneling, which is consistent with the proposed model.

3.2 DEGRADATION OF CHANNEL–CARRIER MOBILITY AT THE SiC–SiO_2 INTERFACE: A CRITICAL OVERVIEW

The extremely low inversion channel-carrier mobility leading to the high channel resistance in N-channel SiC MOSFETs is commonly attributed to a high density of electrically active defects located at or near the SiC–SiO_2 interface. The electrical properties of the SiC–SiO_2 interface are routinely evaluated by conventional methods based on C–V and G–V measurements on MOS capacitors and the underlying theory developed from Si–SiO_2 technology. However, the inherently wide bandgap of SiC results in a broad variation of interface trap response times and therefore, conventional measurements performed at room temperatures can only determine the interface trap density distribution in a relatively narrow energy range, close to the majority carrier band edge [1-4]. The range of analysis can be extended to include deeper levels and approach the midgap by performing the measurements at elevated temperatures; however, it is not possible to examine the D_{it} over the entire bandgap using a single measurement technique on a single substrate type.

Early admittance measurements on as-oxidized P-type SiC–SiO_2 MOS capacitors revealed that the interface trap density was indeed much higher than that frequently observed in as-oxidized SiC–SiO_2 interfaces [5]. Given that N-channel MOSFETs are fabricated on P-type substrates, it was initially considered that the excessive D_{it} observed in the lower half of the SiC bandgap was the primary cause of the severe inversion channel-carrier mobility degradation in SiC MOSFETs. Through incremental advances in surface cleaning and oxidation techniques, the average D_{it} in the lower half of the bandgap in both 4H– and 6H–SiC polytypes was progressively reduced from the high-10^{11} cm^{-2} eV^{-1} range to the low-10^{11} cm^{-2} eV^{-1} range, approaching mid-10^{10} cm^{-2} eV^{-1} values near the midgap [1, 6-8]. It was felt that the SiC–SiO_2 interface was approaching device-grade quality as these

levels were approaching that observed in modern as-oxidized silicon MOS technology. However, there seemed to be little correlation between the evaluation of the interface properties in P-type MOS capacitors and the inversion channel-carrier mobility in SiC MOSFETs [9]. Moreover, the remarkably similar D_{it} observed in the lower half of the bandgap could not explain the apparent polytype dependence on the channel-carrier mobility. In 4H–SiC devices, the reported channel-carrier mobility generally remained below 10 cm^2/Vs [10-12] whereas lateral 6H–SiC devices, fabricated under identical conditions, demonstrated channel-carrier mobilities roughly an order of magnitude higher (~30 – 70 cm^2/Vs) [2, 6, 13, 14], despite possessing roughly half the bulk electron mobility of 4H–SiC. These rather surprisingly results highlighted the fact that a more thorough analysis of the SiC–SiO_2 interface was required in order to gain further insight on the dominant electrically active defects responsible for severely degrading the performance of SiC MOS devices.

Afanasev *et al.* [15] were able to identify a broad distribution of acceptor type near-interfacial oxide traps (NITs) situated approximately 2.8 eV below the SiO_2 conduction band edge in a number of common SiC substrates by investigating the photon-stimulated tunneling of electrons into the oxide. This observation led to the hypothesis that these NITs could contribute to the SiC–SiO_2 energy spectrum by trapping electrons from the inversion layer in N-channel SiC MOSFETs and could be responsible for the severe degradation of the channel-carrier mobility [16]. Since the energy level of these defects corresponds to 0.1 eV below the 4H–SiC conduction band minima (E_C) and therefore within the bandgap of the polytype, these traps were deemed to be particularly detrimental to the electron transport in 4H–SiC inversion layers compared to other SiC polytypes with narrower bandgaps and greater conduction band offsets. Schorner *et al.* [14] arrived at a similar proposition by attributing the polytype influence on the channel-carrier mobility to a broad, high density of acceptor type traps that are

energetically pinned above the valance band edge (E_V) in a number of SiC polytypes as illustrated in Fig. 3.1.

According to Schorner *et al.* [14] the energy position of the broad distribution of acceptor-like traps is believed to peak just below the 4H–SiC conduction band edge. Therefore, a majority of the traps are located above the bandgap of other polytypes where they are considered to be electrically inactive, consequently minimizing their effect. The proposed model tends to provide a qualitative explanation for the observed channel-carrier mobility reduction with the decreasing SiC–SiO_2 conduction band offset (3C → 15R → 6H → 4H) [13, 14, 17].

The interface trap distribution over the entire SiC bandgap can be obtained by measuring the C–V and G–V admittance response of both N- and P-type MOS capacitors over a wide range of temperatures and

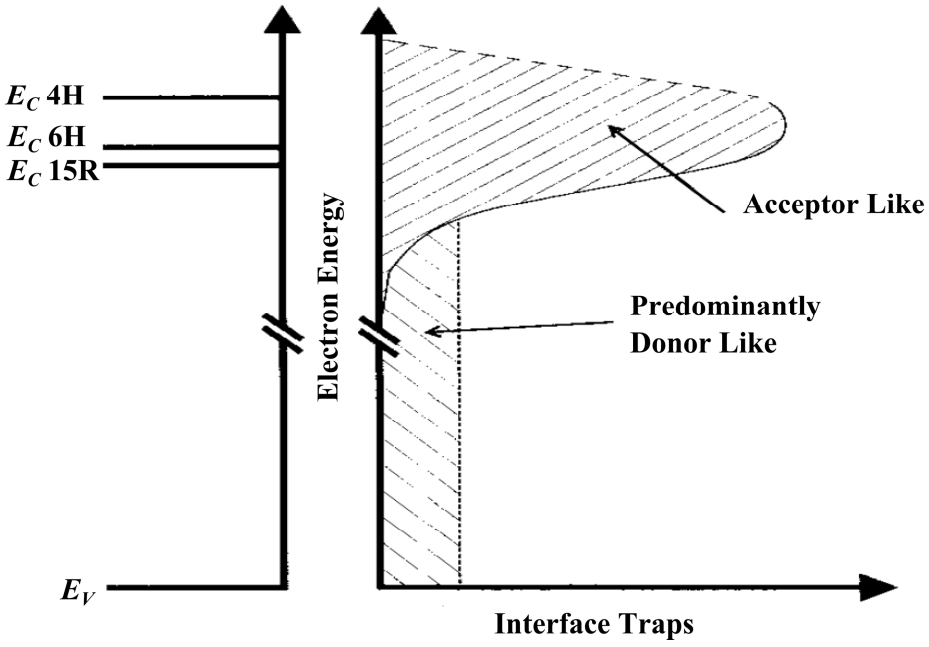

Figure 3.1 Qualitative representation of the interface trap distribution at the SiC–SiO_2 interface for 4H–, 6H– and 15R–SiC polytypes [14].

frequencies. As shown in Fig. 3.2, the interface trap density exponentially increases toward the conduction band edge in as-oxidized 4H– and 6H–SiC *n*-type MOS capacitors [16, 18]. The *shallow* D_{it} near E_C is typically an order of magnitude higher in 4H–SiC (~10^{13} cm^{-2} eV^{-1}) compared to 6H–SiC (~10^{12} cm^{-2} eV^{-1}), which is consistent with the proposed distribution of interface traps. These shallow acceptor-type traps are considered to have a two-fold effect on the conduction properties of the inversion layer channel [18-21]. Primarily, a substantial fraction of mobile electrons become "t*rapped*" in interface states and screen the gate-induced charge. Hence, a larger gate voltage change is required to produce a corresponding change in the

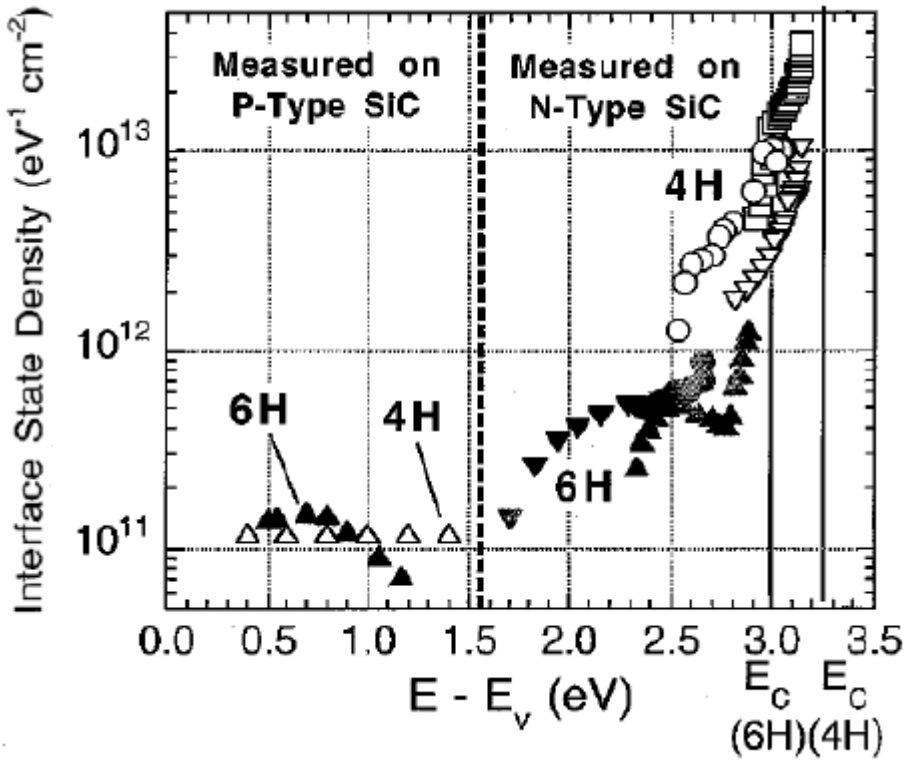

Figure 3.2 Typical interface trap distribution in as-oxidized 4H–SiC (open symbols) and 6H–SiC (closed symbols) obtained by C–V (triangles) and G–V (circles and squares) admittance measurements on N- and P-type MOS capacitors [18].

inversion layer charge. Furthermore, the occupied traps give rise to Coulomb-scattering-limited transport in the inversion channel, reducing the mobility of the remaining free electrons at the $SiC–SiO_2$ interface. These combined effects are typically held accountable for the high threshold voltages and the low channel-carrier mobility frequently observed in 6H– and particularly, 4H–SiC MOSFETs.

The incorporation of nitrogen at the SiC/SiO_2 interface either by direct oxide growth or post-oxidation annealing (POA) in NO or N_2O remains the most popular and widely practiced method in reducing the shallow D_{it} near the 4H–SiC conduction band edge ($E_T \leq 0.2\ eV$) to date. It has been routinely shown that the use of NO typically reduces the shallow D_{it} by roughly an order of magnitude, which generally corresponds to an order of magnitude improvement in the channel channel-carrier mobility [11, 22-24]. Other methods such as the use of phosphorus to "dope" the oxide as pioneered by D. Okamoto et al [25] and the oxidation of SiC in the presence of alkali ions [26-27] have also shown to reduce the shallow D_{it} and significantly enhance the channel-carrier mobility, although it is still unclear if either of these methods is industrially viable. Irrespective of the oxidation method used the channel-carrier mobility still remains a mere fraction of the SiC bulk carrier mobility apparently due to a high density of electron traps located near the 4H–SiC conduction band edge. Therefore the evaluation of D_{it} in close proximity to E_C on N-type MOS capacitors has become the mainstay of current research efforts. However, a universal correlation between the channel-carrier mobility and the shallow interface trap density in SiC MOS devices has not always been observed [28-30].

It is generally recognised that the interface trap response time exponentially decreases towards the majority carrier band edge according to the widely-used Shockley-Read-Hall statistics. Consequently, the accurate evaluation of D_{it} becomes exceedingly more challenging toward E_C

particularly using standard (0.1 – 1 MHz) high-frequency C–V measurements at room temperature, despite of the more apparent impact on the inversion channel-carriers in SiC MOSFETs. From the frequency dependence of the capacitance measured up to 100 MHz it has been observed that SiC–SiO_2 interface traps can still respond measurement frequencies well above 1 MHz [31]. Thus the assumption that 0.1 – 1 MHz AC signals constitute a true high frequency C–V reference measurement becomes invalid as the semiconductor capacitance still includes partial response from the interface traps near E_C. This implies that the interface trap density is underestimated in commonly employed high-low and Terman interface characterisation methods [4]. Consequently it has been proposed that much higher frequencies are required to further enhance the accuracy of estimating the density of shallow SiC–SiO_2 interface traps using such methods [31]. Alternatively, low measurement temperatures have been employed to effectively increase the trap response time and enhance the accuracy of evaluating the D_{it} energetically located near E_C using more practical measurement frequencies [17, 32, 33]. The major deficiency of capacitance based methods however, remains the inability to determine the average capture cross section of the defect for a given energy level and measurement temperature that is required to determine the actual trap emission rate given by SRH theory. Without the capture cross section there is no direct means to establish the range over which the C–V data is precisely valid. This issue can be avoided by employing characterisation techniques that can directly determine the trap response time by resolving the capture cross section such as the AC conductance method.

The capture cross section (σ) defines the average physically active area of a defect centre. If a free electron is found in the vicinity of the defect area it will have a very high probability of capture [34]. The extracted capture cross sections for the most relevant trap levels in Si based MOS devices typically ranges from ~10^{-14} cm^2 to 10^{-16} cm^2 [35-37]. Taking into account that

the physical area of an atom (roughly 10^{-15} cm^2), the possibly charge nature of the defect centre and atomic screening effects, these values are in good agreement with SRH model based on the thermal capture/emission process. In contrast, the reported capture cross sections obtained from AC conductance measurements corresponding to the dominant trap distribution near E_C in 4H–SiC MOS devices are typically much smaller, in the range of 10^{-18} to 10^{-20}cm^2 [38-40]. Other groups employing methods such as constant-capacitance deep level transient spectroscopy (CCDLTS) have also extracted even smaller capture cross sections in the order of 10^{-20} to 10^{-21} cm^2 [41]. While these estimates of σ may satisfy the conventional SRH model mathematically, it becomes obvious that they are far too small to represent any physical significance. The wider implication of this discrepancy is that the high density of traps in close proximity to the 4H-SiC conduction band are simply far too shallow to be conventional interface traps with response times governed by a thermal emission process.

Historically, it has been hypothesized that the effective capture cross section of an oxide trap, as viewed by a carrier at the semiconductor surface, is exponentially reduced with the distance the trap is located away from the semiconductor surface [42]. Therefore the significantly small capture cross sections located close to the conduction band edge are considered to be an effect of the near-interface traps spatially located in the transitional region, bordering the SiC–SiO_2 interfaces [41]. This assumption implies that the trap-carrier capture mechanism would also have to involve tunneling mechanisms to form a more complex two-step electron capture and emission process [43-45]. In this process electrons are first emitted from a near-interface traps located in the oxide by tunneling to conventional interface traps of the same energy level followed by thermal emission back into the conduction band. Since the tunneling and SRH processes occur in series the overall trap response time is effectively increased, therefore making it realistically possible for shallow interface states to respond to

practical measurement signal periods. The application of a two-step carrier-trap transport mechanism is consistent with the perception that NITs are the dominant trap type in 4H-SiC MOS devices. This also emphasizes the fact that the electrical characteristics of the SiC–SiO_2 interface significantly deviates from the model developed for the well-known Si–SiO_2 interface. Therefore ambiguity is to be expected when the density of NITs near E_C in SiC MOS structures is evaluated using conventional techniques that are based on the statistical model which was explicitly developed to describe the behaviour of interface traps governed by a thermal activated transport process.

The channel-carrier mobility remains one of the most highly reported figures of merit for the performance of SiC power MOSFETs to date. However, this parameter does not provide comprehensive details of the electron transport process in the inversion layer and can be subject to misinterpretation. The peak channel-carrier mobility is commonly acquired from the highest transconductance ($g_m = \partial I_D/\partial V_G$) that is extracted from the steepest part of the measured MOSFET $I_D - V_G$ transfer characteristic using the following expression [46],

$$\mu_{ch} = \frac{L(\partial I_D/\partial V_G)}{W C_{ox} V_{DS}} = \frac{\partial \sigma/\partial V_G}{C_{ox}} \tag{3.1}$$

where (L/W) is the geometric length to width ratio of the inversion channel, C_{ox} is the oxide capacitance, V_{DS} is the drain to source voltage, V_G is the applied gate voltage, and

$$\sigma = q\mu_{inv} n_{inv} \tag{3.2}$$

is the conductivity of the inversion layer. Hence the channel-carrier mobility is proportional to the electron concentration (n_{inv}) and the average mobility of these electrons in the inversion layer (μ_{inv}). It is frequently

assumed that the total density of electrons in the inversion layer can be approximated by charge sheet model

$$n_{inv} = Q_{inv}/q = C_{ox}(V_G - V_T)/q \tag{3.3}$$

where Q_{inv} is the inversion layer charge density, V_T is the threshold voltage and q is the unit electron charge. In state of the art silicon MOSFETs, where the effects of interface traps are generally considered negligible, Eq. (3.3) can accurately estimate n_{inv} as a function of V_G and accordingly, μ_{ch} is approximately equal to the actual electron mobility in the inversion channel. However, in SiC–SiO_2 interfaces, where the observed density of acceptor-type traps is relatively high near E_C, n_{inv} can be much lower than predicted from Eq. (3.3). Consequently, the channel-carrier mobility extracted from the transfer characteristics of SiC MOSFETs can provide misleading information on the inversion layer electron transport properties if it is assumed to be equal to the actual electron mobility in the channel [19]. On the contrary, Hall measurements can be used to independently resolve the free electron density and the electron mobility in the inversion layer, irrespective of the interface trap density. Another major advantage of the Hall technique is that MOS Hall structures can be fabricated on the same substrates as N-channel MOSFETs, and by using this data, the dominant factors responsible for impeding the electron transport in MOS inversion layers can be directly inferred.

Saks *et al.*[19, 47] initially demonstrated the effects of charge trapping on the electron transport in SiC inversion layers using the Hall effect technique. These experiments revealed that the Hall mobility in gated SiC structures is much larger than the channel-carrier mobility extracted from the SiC MOSFET transconductance data and that the free electron concentration is much smaller than the expected number of inversion layer electrons predicted by Eq. (3.3), indicating that electron trapping at the SiC–

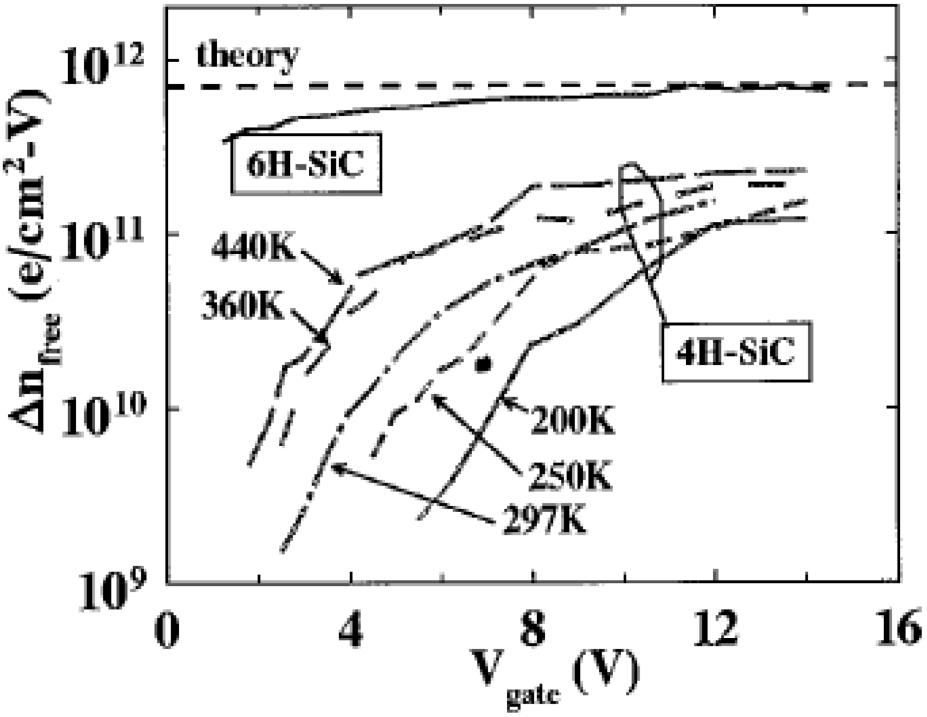

Figure 3.3 The change in the free electron density per volt change in the gate voltage (Δn_{free}) obtained from Hall measurements in as-oxidized 4H– and 6H–SiC MOS devices. The significant discrepancy between the experimental and maximum theoretical value of Δn_{free} even at high gate voltage highlights the severity of inversion layer electron trapping in 4H–SiC devices [19].

SiO_2 interfacial region severely affects these devices. The free electron densities (n_{free}) obtained from these Hall measurements for 4H– and 6H–SiC MOS devices fabricated by conventional oxidation processes are shown in Fig. 3.3 [19]. The maximum theoretical inversion electron concentration in the absence of electron trapping is given by Δn_{total} (= C_{ox}/q), to avoid discrepancies obtaining a well-defined value for $V_{T,}$ is compared to the experimentally derived free electron change per volt change in the gate voltage Δn_{free} (= $\partial n_{free} / \partial V_G$) as a function of the applied gate voltage. For the 6H–SiC device it is shown that Δn_{free} approaches the theoretical value when V_G is well beyond threshold. In contrast, Δn_{free} in the 4H–SiC device

remains well below theory, even under strong inversion conditions. At the highest gate voltage it has been estimated that a substantial fraction (~80%) of inversion layer electrons are trapped and cannot contribute to the conductance in the channel of 4H–SiC MOSFETs. It has also been reported that a large fraction (~50%) of inversion electrons remain trapped even after state of the art gate oxide nitridation [20, 48, 49]. Moreover, it has been shown that the severity of electron trapping in 4H–SiC inversion layers continues to increase with the applied gate voltage above threshold and does not appear to saturate [20, 48, 49]. These Hall measurements therefore suggest that the transconductance and channel-carrier mobility in 4H–SiC MOSFETs is in fact dominated by the substantial reduction of the free electron concentration in the inversion channel under strong inversion conditions unlike the scattering mechanisms that dominate the channel-carrier mobility in modern Si MOSFETs, which is comparatively high.

3.3 CHARACTERISATION OF THE ACTIVE NEAR-INTERFACE TRAPS BASED ON ACCUMULATION CONDUCTANCE MEASUREMENTS

In spite of compelling experimental Hall results, the 4H–SiC/SiO_2 interface is still routinely evaluated by obtaining the density of NITs near E_C from conventional MOS admittance measurements of N-type MOS capacitors in *depletion*. The energy levels of these NITs would correspond to an N-channel MOSFET biased to cut-off or generally speaking, "*off*" mode ($V_G < V_T$) and can therefore influence the threshold voltage and turn on characteristics of a MOSFET due to the contribution of the trapped charge in the occupied near-interface traps (Q_{NIT}). Considering these NITs are active below threshold biases, they bare little influence on the free electron concentration in the inversion layer and consequently, the low channel-carrier mobility that is extracted from the measured MOSFET transconductance when biased to *strong inversion* ($V_G >> V_T$). The effects of

the NITs located both in depletion and strong inversion on the total inversion electron density modelled by Eq. (3.3) are schematically represented in Fig. 3.4. This figure clearly demonstrates that NITs with energy levels corresponding to strong inversion are responsible for the behaviour observed in 4H–SiC inversion layers.

According to classical semiconductor physics, that assumes non-degenerate conditions, the Fermi level corresponding to strong inversion is located very close to but at least a few kT below the conduction band edge of the semiconductor band-gap [37]. This assumption is generally valid for the Fermi level position in MOS capacitors under conventional analysis conditions. In MOSFETs however, the channel is subject to degeneracy under normal operating conditions due to the application of high gate biases. This leads to surface quantization and quantum-confinement of channel carriers in a MOSFET in strong inversion which positions the Fermi level inside the conduction band [50-53].

While it is still possible to explain the occupancy of NITs aligned to the conduction band without surface quantization using the classical approach—where the Fermi level remains well below E_C but the thermal broadening of the Fermi–Dirac (F–D) probability distribution function can allow conduction band trap occupancy—this approach would be less realistic given that the quantum-confinement effects in MOS inversion layers do exist. It therefore becomes important to investigate the NITs with energy levels aligned to the conduction band as they are active and can trap MOSFET channel-carriers in strong inversion. However there are currently no established techniques to characterise the near-interface traps aligned to the conduction band using convenient MOS capacitor structures. Taking into account the relevancy of these traps on the conductivity of 4H–SiC inversion layers, a new technique based on the conductance measurements

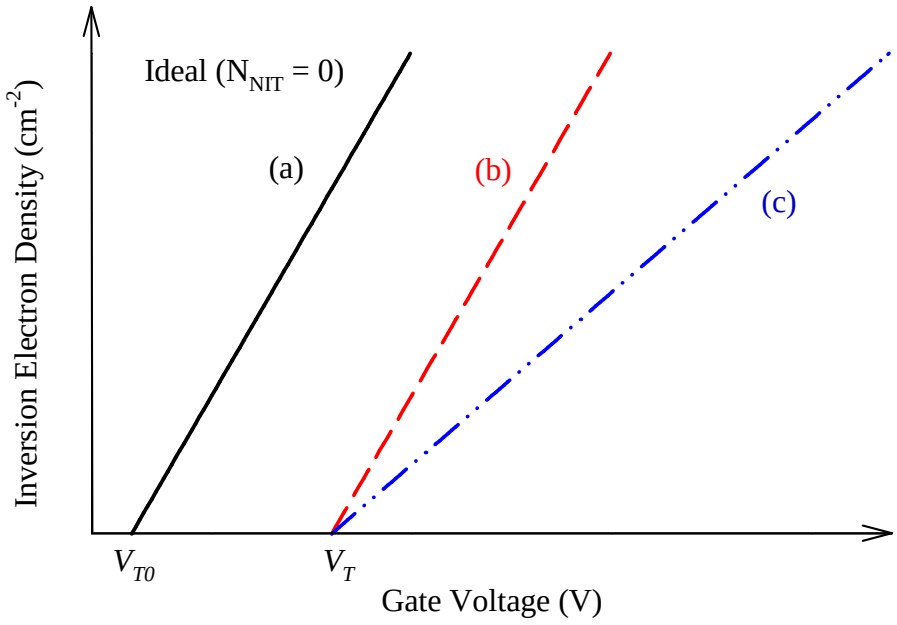

Figure 3.4 A graphical representation of the effects of NITs energetically located in *depletion* and *strong inversion* on the electron density in 4H–SiC inversion layers. The theoretical inversion electron density in the absence of carrier trapping is modelled by curve (a) where N_{NIT} represents the number of near-interface traps. For practical devices, the extracted threshold voltage (V_T) is offset from the ideal (V_{T0}) by the immobile charge trapped in NITs located in depletion. The theoretical relationship between the inversion electron density and the gate voltage is retained beyond threshold if carrier trapping is only limited to energy levels corresponding to depletion (b). However, if carrier trapping also continues to occur in strong inversion (c), the inversion electron density can be significantly reduced. This scenario is representative of the behaviour that is commonly observed in 4H–SiC inversion layers by the Hall technique.

of N-type MOS capacitors biased in accumulation is developed in the following sections.

3.3.1 Identification of the Active Near-Interface Traps: Quantum Confinement Effects in the MOS Inversion Channel

Quantum confinement effects are pronounced in the channel of MOSFETs because of the very high electric fields and, consequently, can induce band-bending strong enough that electrons become confined to a narrow potential well close to the semiconductor surface and their energy is then quantized in the direction normal to the surface [50-53]. This is often referred to as a 2-diamensional electron gas (2-DEG). The quantum confinement of carriers to a potential well that restricts the carrier motion in two dimensions is characterized by quantized two-dimensional energy subbands inside the conduction band [50-54], as illustrated in Fig. 3.5. Given that the bottom of the lowest two-dimensional subband (E_o) is well above the energy that corresponds to the bottom of the three-dimensional conduction band (E_C), the channel electrons do not appear in the two-dimensional subbands until the surface energy bending is so strong that the Fermi level appears well above E_C.

Inversion layer subband structures and quantized energy levels in N-type hexagonal SiC polytypes have been determined by Pennington and Goldsman [55]. Physical models and simulations to quantify quantum confinement effects on 4H-SiC MOSFET conduction-band trap occupancy, employing the density gradient formalism and density functional theory, have been investigated by Potbhare *et al.* [56, 57]. They have shown excellent comparison to experimentally measured MOSFETs with significant differences observed in trap occupancy compared to classical methods and have implied that quantum confinement effects should be considered while evaluating trap distributions.

Considering that the quantum confinement effect sets the Fermi level in strong inversion well above E_C, the electrons from the inversion layer should be able to directly communicate with near-interface traps whose levels are aligned to the conduction band by tunneling. The theory behind the capture and emission of majority carriers as a result of near-interface trap located in the oxide in close proximity to the semiconductor surface by quantum mechanical tunnelling has been described in great detail by Heiman and Warfield [41]. The tunnelling model assumes that the interface at $x = 0$ extends into the oxide and border traps or near-interface traps occupy this spatially extended interface. It is considered that the basic physics of the tunnelling model can be retained and the theory simply extended to consider the capture and emission of channel electrons by NITs aligned to the conduction band. This implies that the conventional model,

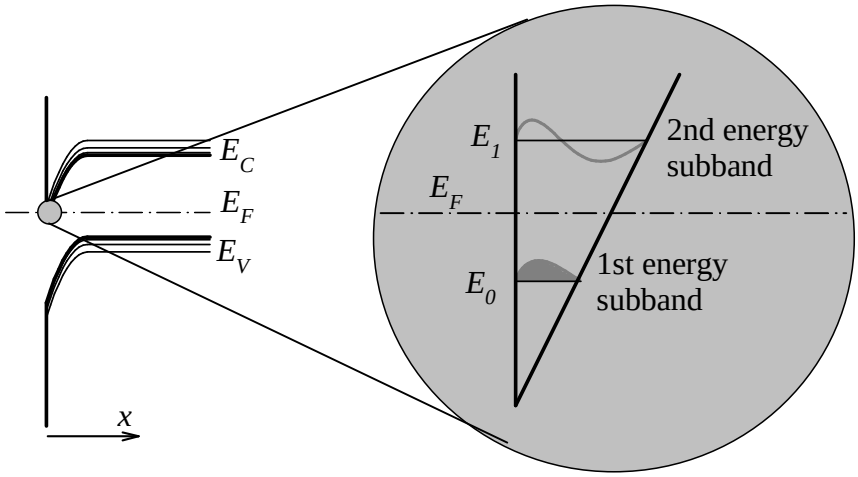

Figure 3.5 Illustration of the quantum well and the formation of the two-dimensional subbands in a strongly inverted semiconductor surface. The Fermi level (E_F) appears above the bottom of the first energy subband (E_0) and well above E_C (the bottom of the triangular potential well) [51].

based on thermal capture and emission of charge carriers, is unrelated to the electrically active NITs in 4H–SiC inversion layers. Figure 3.6a illustrates these effects on a strongly inverted P-type substrate that forms the N-type conductive channel in a SiC MOSFET. The Fermi level is positioned above E_C at the SiC–SiO_2 interface due to the additional band bending caused by the quantum confinement of electrons. Any NITs with energy levels below the Fermi level have a high probability of electron occupancy. These trapped electrons are, therefore, unavailable for channel conduction.

The inversion channel should be highly conductive due to the high density of states in the two-dimensional subbands, however this is not observed in 4H-SiC MOSFETs. The most likely scenario is that the density of NITs with energy levels below the Fermi level becomes comparable to the density of states in the subbands. This scenario becomes very plausible, considering that a large density of NITs is commonly reported to exist near the 4H-SiC conduction-band edge [58]. If the majority of electrons drawn to the SiC–SiO_2 surface are captured by NITs with energy levels below the Fermi level, the density of electrons remaining in the conduction subbands in the inversion channel is significantly reduced. Therefore the transconductance that is frequently used to calculate the average channel-carrier mobility for the total charge attracted by the gate voltage is also substantially reduced as shown in Fig. 3.6a.

Since it is very convenient to fabricate MOS capacitors rather than MOS Hall structures or complete MOSFETs for evaluation of the SiC–SiO_2 interface, it is proposed that these NITs can be detected in conductance measurements on N-type MOS capacitors. Figure 3.6b indicates that the surface region of an N-type MOS capacitor biased well into accumulation is equivalent to the N-channel MOSFET in strong inversion in terms of the possible transfer process between the surface electrons and near-interface traps aligned to the conduction band. This figure also illustrates that the

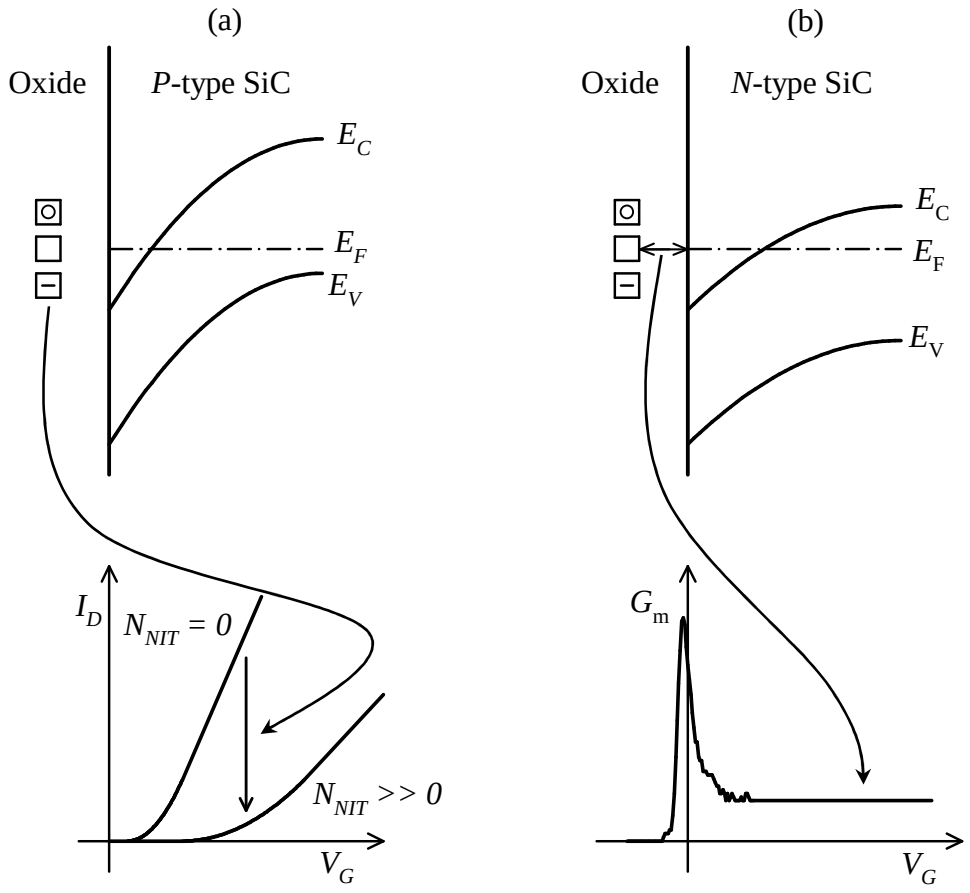

Figure 3.6 The effects of near-interface traps energetically aligned to the conduction band, on (a) an N-channel SiC MOSFET and (b) an N-type MOS capacitor. The Fermi level enters the conduction band in the band diagrams due to the effects of quantum confinement. N_{NIT} denotes the number of near-interface traps.

carrier-trap transfer process is related to the measured conductance (G_m) in accumulation that has been experimentally observed in SiC MOS capacitors [59, 60]. To enable the conductance measurements, a small AC signal is superimposed to the DC bias. This oscillates the energy levels of the NITs above and below the Fermi level, which results in electron capture from and release into the channel by tunneling. The measured conductance in accumulation can therefore be considered as a direct result of the capture and release of these electrons.

3.3.2 Experimental Details

MOS capacitors were fabricated on N-type, Si-face (0001), 4H–SiC epitaxial substrates purchased from CREE Research Inc. (USA). The 5 μm epitaxial layer was doped with nitrogen to a concentration of $\approx 10^{16}$ cm^{-3}. All samples were prepared using a Radio Corporation of America (RCA) cleaning procedure, followed by immersion in 10% hydrofluoric acid (HF) for 5 minutes to remove any native oxides prior to oxidation. The gate oxide was thermally grown in an atmospheric SiC tube furnace at 1250°C using a NO-nitridation "sandwich" type process [23] to provide a reasonable $SiC–SiO_2$ interface. Aluminium was sputter deposited on the oxide and defined by photolithography to form square gate contacts with an area of $0.0025cm^2$. Aluminium was also deposited on the back of the substrate to form a large area ohmic contact.

High-frequency capacitance-voltage and conductance-voltage measurements were performed using a HP 4284A precision LCR meter under a light-tight and temperature controlled probe station. The MOS capacitors were swept from strong accumulation to deep depletion by applying gate biases between ± 10 V, superimposed with an AC signal of 50 mV amplitude. A slow sweep rate of 0.1V/s was applied to allow equilibrium between the trap states and the DC component. The measurement frequency was between 1 kHz to 100 kHz at both 25°C and 200°C to examine the frequency dispersion and temperature dependence of the NITs. The gate-oxide thickness was approximately 50 nm as determined from the accumulation capacitance of the 1 kHz curve with a relative dielectric constant of 3.9. To designate the onset of accumulation in both the C–V and G–V curves the flatband condition ($\varphi = 0$) was determined by calculating the flatband capacitance and ascertaining the corresponding flatband voltages using the methods outlined in Chapter 2. The effective interface

trapped charge (Q_{it}) was determined by the flatband-voltage shift (ΔV_{FB}) between the 1 kHz to 100 kHz C-V curves from the following expression

$$Q_{it} = \frac{C_{ox}\,\Delta V_{FB(1-100\,kHz)}}{qA} \tag{3.4}$$

where A defines the gate area, q is the electron charge and C_{ox} the oxide capacitance measured in accumulation.

3.3.3 Detection of the Active Near-Interface Traps: Measurements of the MOS Conductance in Accumulation

A typical set of high-frequency C–V and G–V curves obtained from a 4H-SiC MOS capacitor measured at 10 kHz and room temperature (25°C) is shown in Fig. 3.7. The observed conductance peak indicates a resonant trap-carrier response in depletion that corresponds to conventional theory, based and thermally activated transport. In addition, substantial measured conductance is still present when the gate voltage biases the capacitor into the accumulation regime. These characteristics are very similar to that previously reported in the literature [17, 59, 60]. The fact that the measured AC conductance in accumulation does not drop to zero level indicates the suspected presence of near-interface traps aligned to the conduction band.

To verify this conclusion, the DC conductance was measured and found to be at low ρA values, close to measurement noise levels. This indicates that the AC accumulation conductance is not due to oxide leakage or Fowler-Nordheim tunneling. The observed bias independence of the measured conductance in accumulation can be explained by the effective *pinning* of the Fermi level. Once Fermi level enters the conduction band the influence of additional gate bias on the band bending will becomes quite minor as it is dropped across the oxide.

Clearly, the capture and the release mechanism of electrons by these NITs corresponding to a relatively long measurement frequency period of 100 μs would have to occur by tunneling. The statistical model based on the SRH thermal emission process can be ruled out simply because the response times of these states aligned to the conduction band would be virtually instantaneous and would therefore be immeasurable under this measurement frequency period.

The minimal frequency dispersion of the C–V curves shown in Fig. 3.8 tends to indicate that the oxide quality is quite reasonable, as would be expected from an NO based oxidation process. This is reflected in the rather small effective interface trapped charge of 2.3×10^{-10} cm^{-2} based on the C–V curve stretch out measured at flatband using Eq. (3.4). On the other hand,

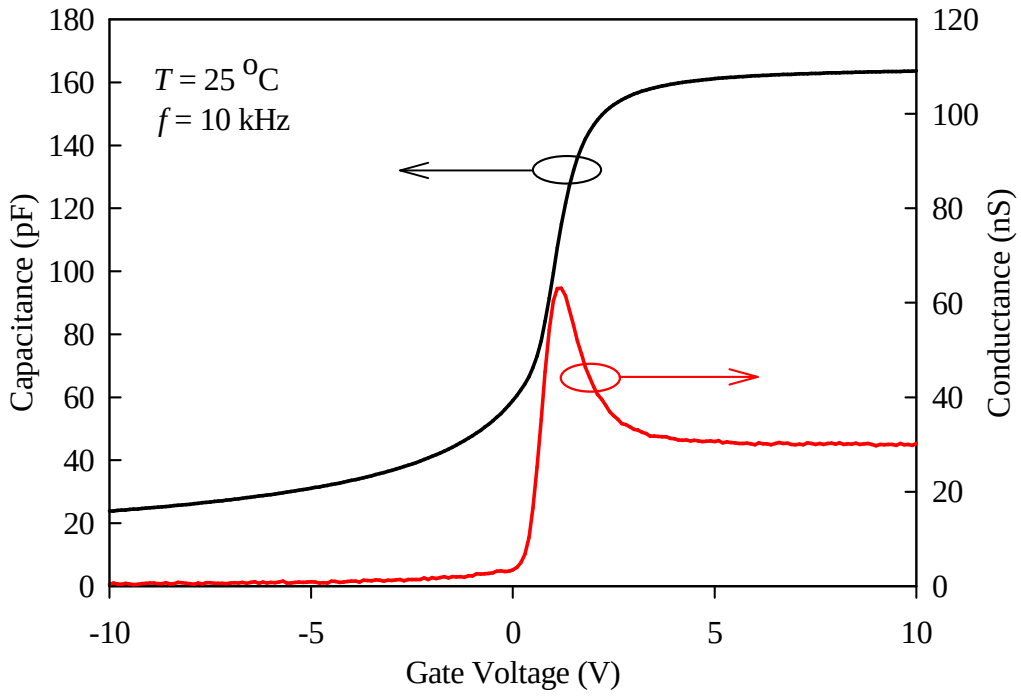

Figure 3.7 Capacitance–voltage and conductance–voltage characteristics of an N-type 4H–SiC MOS capacitor measured at 10 kHz and 25°C.

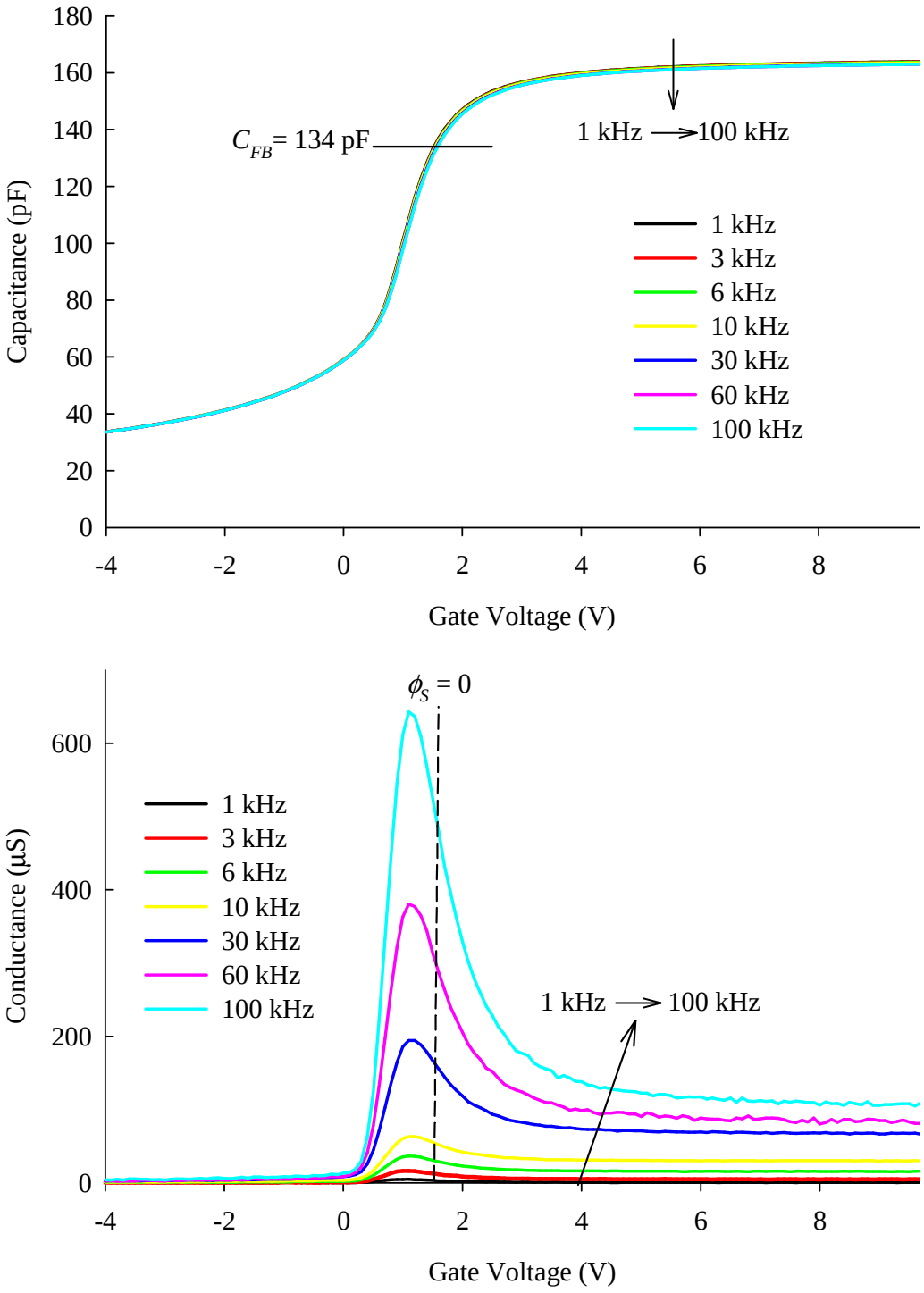

Figure 3.8 Frequency characteristics of capacitance-voltage and corresponding conductance voltage curves measured at 25°C. Significant frequency dispersion of the conductance measured in strong accumulation ($V_G \geq$ *6 V*) is observed indicating the presence of NITs aligned to the conduction band.

the conductance measurements, renowned for sensitivity, clearly display frequency dispersion in depletion, as would be expected using conventional analysis techniques. Likewise, the conductance measured in strong accumulation[1] ($V_G > V_{FB}$) also exhibits frequency dispersion. This observation cannot be explained by conventional circuit models. Provided the carrier-NIT transport is due to direct tunneling, then the frequency dependent accumulation conductance will correspond to the carrier tunneling time and therefore will be directly related to the average tunneling distance between the NITs and the SiC surface. This hypothesis is consistent with the physics behind the tunneling model [42]. In accordance with the tunneling model, the observed frequency dependent rise in the

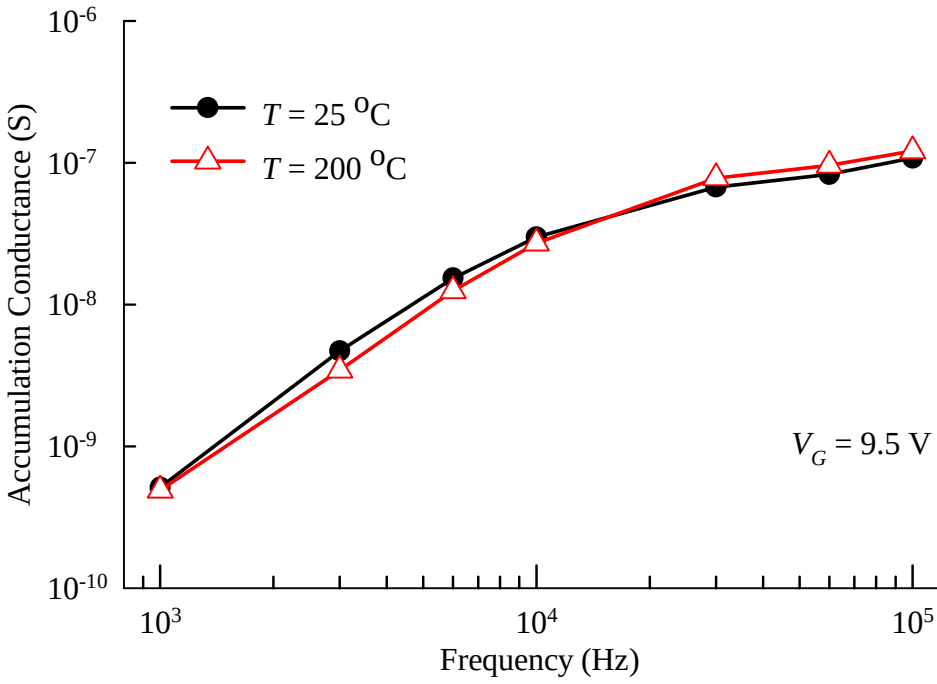

Figure 3.9 The conductance measured in 4H–SiC MOS capacitors at 25 °C and 200 °C corresponding to a gate bias well into accumulation ($V_G = 9.5V$). The Temperature independence indicates that the carrier-NIT transport mechanism is due to tunneling.

accumulation conductance implies that the density of NITs increases towards the SiC surface (x → 0). The NITs with shorter tunneling distances will consequently exhibit shorter carrier-NIT response times and therefore respond to higher measurement frequencies.

In full accordance to pure tunneling transport mechanism, the accumulation conductance must be independent of temperature. A comparison of the conductance measured in strong accumulation (V_G = 9.5V) at 25 °C and 200 °C as a function of frequency is presented in Fig. 3.9. These results reveal no temperature dependencies that indicate the presence of thermal emission and therefore demonstrate that the accumulation conductance is due to temperature-independent tunneling of electrons to NITs aligned to the conduction band which is in full agreement with the presented model.

3.3.4 The Conductance Measured in Accumulation: Effects of Series Resistance

The source of any measured small-signal energy loss of a MOS capacitor biased in accumulation is generally considered to be an artefact, exclusively due to the parasitic effects of series resistance and not due to the effects of charge-carrier trapping according to conventional theory. Series resistance arises from both intrinsic and extrinsic sources. The major contributors consist of: the resistance between the back contact and the space-charge region of substrate bulk under the gate; the resistance of gate and back contacts; and the resistance associated with the measurement equipment. The conventional approach is to obtain the series resistance from the measured admittance response of a MOS capacitor and apply a correction factor to in order to avoid its influence on the quantification of the interface trap density. The equivalent circuit models of a MOS capacitor including the parasitic series resistance (R_S) are shown in Fig. 3.10. Figure 3.10a indicates that the series resistance can impact both the overall measured

capacitance and the measured conductance of a MOS capacitor in depletion.

The greatest influence of the series resistance on the measured parameters is considered to occur in strong accumulation [37]. The equivalent circuit of a MOS capacitor biased to accumulation is displayed in Fig. 3.10b, where the accumulation layer capacitance (C_A) is now in parallel with the *RC* series trap admittance network (Y_{it}). Since C_A is large, the trap admittance becomes negligible according to expressions given by Lehovec [61, 62]. Therefore, C_A effectively shunts Y_{it} and the equivalent circuit becomes that of Fig. 3.10c. The equivalent circuit of the MOS capacitor in strong accumulation can be further simplified to C_{ox} in series with R_S because $C_A \gg C_{ox}$, as shown in Fig. 3.10d. The parasitic series resistance can be determined from of the measured accumulation capacitance (C_{ma}) and measured accumulation conductance (G_{ma}) from this circuit model by the following expression:

$$R_S = \frac{G_{ma}}{{G_{ma}}^2 + (\omega C_{ma})^2} \tag{3.5}$$

The capacitance and conductance measured from the MOS capacitor can be both corrected once R_S is obtained.

The previous section has shown that 4H–SiC MOS capacitors exhibit significant conductance in accumulation (Fig. 3.8). However, according to the equivalent circuit model in Fig. 3.10d, the effects of carrier trapping in accumulation should not be present in the measurement for interfaces that cohere to Lehovec's expressions. Therefore, the measured conductance in accumulation would typically be considered an effect of the parasitic series resistance and disregarded by applying correction factors obtained from Eq. (3.5). In practice this resistance should only be in the order of an ohm or so. However, if R_S is calculated from these measurements it becomes

unrealistically high (R_S ≈ 500Ω @ 1kHz and R_S ≈ 12Ω @ 100kHz). Furthermore is also becomes dependent on the measurement frequency. The frequency dispersion of R_S however is not expected according to the equivalent circuit model.

These discrepancies tend to suggest that conventional equivalent circuit model cannot be used to explain the conductance observed in 4H–SiC MOS capacitors biased to accumulation. Therefore it becomes highly improbable that the accumulation conductance in 4H–SiC MOS capacitors is exclusively due to the effects of parasitic series resistance. On the other hand, if quantum confinement effects are considered and the Fermi level is aligned to the conduction band, then the proposed hypothesis that entails

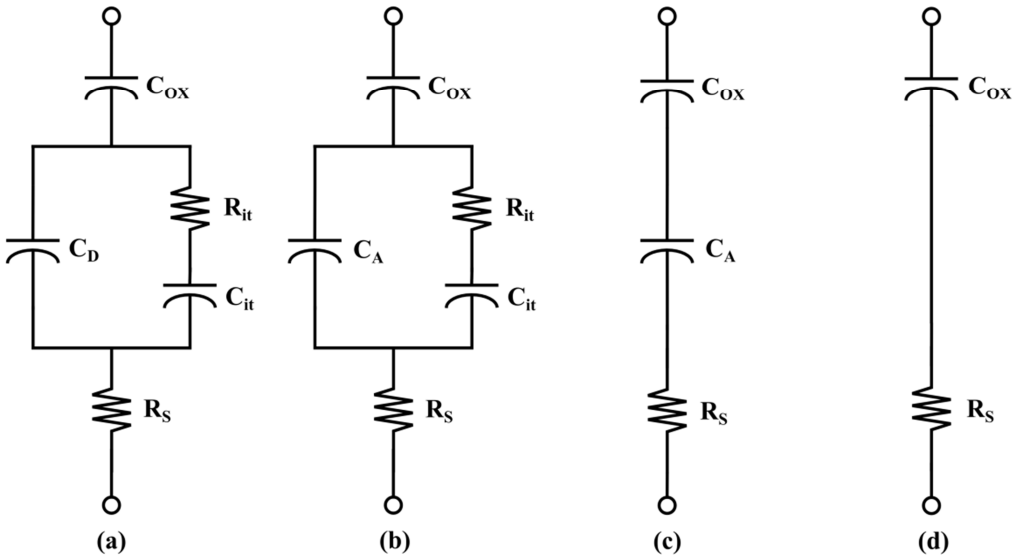

Figure 3.10 (a) Equivalent circuit model of a MOS capacitor including parasitic series resistance (R_S) in depletion; (b) Equivalent circuit of a MOS capacitor in strong accumulation; (c) Simplified model of (b); (d) Simplified model of (c) used to extract the parameters C_{ox} and R_S in strong accumulation [34].

the trapping/detrapping of electrons in near-interface traps spatially located in oxide by tunneling can offer a plausible explanation for the frequency dependent behaviour of the measured accumulation conductance that is observed in these devices.

SUMMARY

The effects of carrier trapping at the SiC–SiO_2 interface on the electrical characteristics in 4H–SiC MOSFETs have been critically reviewed in this chapter leading to a novel understanding and detection method of the electrically active NITs that dominate the channel-carrier mobility in these devices.

Based on a review of the current literature, it is generally accepted that a large density of traps energetically located near the 4H–SiC conduction band minima are responsible for the severe degradation of channel-carrier mobility in 4H–SiC MOSFETs. Conventional interface characterisation techniques based on C–V and G–V measurements of N–type MOS capacitors are routinely employed to evaluate the density of these defects located in close proximity to the conduction band edge. However, applying the Shockley-Read-Hall statistical model to these shallow states yields unrealistically small capture cross section values. This implies that the electrically active defects near E_C are far too shallow to be conventional interface traps with response times exclusively modelled by thermally activated transport. To explain the longer than expected response time these defects are believed to be near-interface oxide traps that communicate with conduction band electrons through a combined thermal-tunneling process. However the statistical model was never explicitly developed to investigate the behaviour of NITs. Therefore ambiguity is to be expected in the characterisation of NITs in SiC MOS devices using conventional techniques.

A review of Hall measurements reported in the literature has revealed that the channel-carrier mobility in 4H–SiC MOSFETs is, in fact, dominated by the substantial reduction of the free electron concentration in the inversion channel. Moreover, it has been shown that the severity of electron trapping continues to increase linearly as a function of the applied gate voltage. Despite these outstanding results that directly link the low channel conductance to the significant electron trapping under strong inversion conditions, the focus of current research still remains in the evaluation of the NITs near the conduction band edge from C–V and G–V measurements of N–type MOS capacitors biased in depletion. Using the charge sheet model it was empirically demonstrated that the NITs corresponding to gate biases in depletion can only influence the threshold voltage and turn on characteristics of a MOSFET as a result of the charge in the occupied traps. However they are not responsible for reducing the inversion layer electron concentration beyond threshold that is experimentally observed in 4H–SiC MOSFETs.

Because of very strong band bending and the quantum confinement of carriers that exists in the inversion channel of a MOSFET, the Fermi level enters energy levels above the bottom of the conduction band and therefore, the existence of NITs with energy levels aligned to the conduction band have been proposed as the main impacting factor on the channel-carrier mobility in 4H–SiC MOSFETs, as opposed to traps residing in the SiC energy gap. This coincides with the concept that the electrons in the inversion and accumulation layers can directly tunnel to and from NITs with energy levels above the bottom of the conduction band.

It has been experimentally demonstrated that conductance measurements of N-type MOS capacitors biased in accumulation can be used as a direct method to detect and characterise these NITs [63]. This is possible because the surface region of the energy band diagram of an MOS

capacitor in accumulation is distinctly similar to that of an N-channel MOSFET in strong inversion. Measurements carried out on 4H–SiC MOS capacitors have shown that the accumulation conductance shows no temperature dependence to suggest thermal emission, therefore confirming that direct tunnelling is the responsible mechanism for capture of channel electrons by these NITs. The frequency dependence of the accumulation conductance indicates that the NIT density significantly increases closer to the SiC–SiO_2 interface due to shorter carrier–NIT tunneling distances and therefore shorter tunneling times, increasing the accumulation conductance at higher measuring frequencies.

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4

NITRIDATION OF THE SiC–SiO_2 INTERFACE AT LOW PARTIAL-PRESSURE

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4.1 INTRODUCTION

The growth of high quality gate oxide insulation layers combined with abrupt SiC–SiO_2 interfaces, containing a low density of electrically active defects, is crucial for the fabrication of commercially viable SiC surface-sensitive, MOS-based, semiconductor devices. While the thermal oxidation of SiC through conventional dry or wet oxidation techniques yields a high quality silicon dioxide insulation layer, identical to that of the highly successful Si-based MOS technology, the termination of the SiC surface through these processes has proven insufficient, leading to a high density of electrically active defects, extremely low channel-carrier mobility and high channel resistance in SiC MOSFETs. The most significant technological breakthrough towards the recent commercial availability of SiC MOSFETs has been through the incorporation of nitrogen at the SiC–SiO_2 interface via high temperature, gate oxide nitridation in nitrogen containing precursor gas such as nitrous oxide (N_2O) or nitric oxide (NO).

Following a brief review on the oxidation kinetics and defect formation at the SiC–SiO_2 interface, the effects of nitrogen at the SiC–SiO_2 and the development of gate oxide nitridation techniques on SiC are presented in this chapter. Among the various gate oxide nitridation techniques reviewed, gate oxides grown directly in pure NO yield the greatest improvements in the electrical properties of the SiC–SiO_2 interface. However, the extremely slow oxide growth rate, toxicity, and the expense of NO gas makes this process impractical for the growth of thick gate oxides required for the fabrication of SiC power MOSFETs, especially in large, production-type oxidation furnaces due to the sheer volume of gas required to achieve and maintain a pure NO ambient. Given the ever-increasing size of 4H–SiC wafers and thus, the size of the supporting oxidation equipment, it may also become difficult to replicate the exact ambient conditions for conventional gate oxide nitridation by annealing in pure NO that have been

developed in small research-type oxidation furnaces, requiring minimal precursor gas budgets.

To address these issues, the effects of NO-nitridation at a very low partial-pressure on the electrical properties of the 4H–SiC/SiO_2 interface and the integrity of the grown oxide layer are investigated in this chapter. This investigation is realized through the fabrication of MOS capacitors by a sequential gate nitridation/oxidation/nitridation "*sandwich*" type process and a novel, combined nitridation/oxidation process, both employing NO at very low partial pressure in a high-volume, production-based oxidation furnace. It is demonstrated that NO-nitridation at a low partial pressure of only 2 % is still effective at improving the quality of both the 4H–SiC/SiO_2 interface and the grown gate oxide layer, even in the presence of additional O_2.

4.2 AN OVERVIEW OF THERMALLY GROWN SiC GATE OXIDES

The thermal oxidation of SiC yields a stoichiometric SiO_2 oxide layer with bulk properties very similar to that of oxides thermally grown on Si [1]. In the presence of oxygen at high temperature the oxidation of SiC can be determined by the net reaction:

$$2\,SiC + 3O_2 \rightarrow 2\,SiO_2 + 2CO \qquad (4.1)$$

From this reaction it is believed that the oxidation of SiC forms a native SiO_2 oxide layer and a gaseous carbon related by-product (CO) that is considered to out-diffuse through the grown oxide layer to completely remove its presence from the oxide [2, 3]. Although this process grows high quality SiO_2 layers, the electrical properties of the as-oxidized SiC–SiO_2 interface are remarkably poor and far from device-grade quality in comparison to that of conventional Si–SiO_2 interfaces. The density of

electrically active defects at SiC–SiO_2 interfaces immediately after thermal oxidation is routinely around two orders of magnitude higher than that observed in Si MOS technology [4-7]. Ultimately, this excessive density of states significantly reduces the free carrier concentration in the inversion channel and give rises to Coulomb scattering that impedes the mobility of the remaining free carriers. As a combined result of these factors, the channel-carrier mobility in as-oxidized 4H– and 6H–SiC MOSFETs is only a mere fraction of the carrier mobility in the bulk and insufficient for commercial devices; corresponding to only approximately 1 % and 20 % of the bulk respectively [8-12]. In contrast, the channel-carrier mobility in modern, thermally oxidized Si-based devices following hydrogen passivation of the Si–SiO_2 interface typically approaches half that of the carrier mobility in the bulk. Accordingly, research has been focused on investigating the physical origin of the defects located at the SiC-SiO_2 interfacial region and processing techniques to remove or electrically passivated them in order to enhance the channel-carrier mobility in SiC MOSFETs and enable commercial viability.

4.2.1 Electrically Active Defects at the SiC–SiO_2 Interfaces

It is well-known that the lattice mismatch between the silicon and the thermally grown oxide layer gives rise to dangling bonds of surface silicon atoms (P_b-type centres), which are the most influential type of defect at the (111) Si–SiO_2 interface [13]. These P_b centres can be easily *passivated* by hydrogen at moderate temperatures (< 400 ^{0}C) to form electrically inactive Si_3≡Si–H structures and significantly reduce the D_{it} in Si MOS technology [14, 15]. Given that the (111) Si–SiO_2 interface is structurally isomorphic to that of as-oxidised Si faced, hexagonal SiC these Si–dangling bond defects are expected to contribute to the interface trap density spectrum at the SiC–SiO_2 interface. However, in contrast to Si MOS devices, the electrically active defects at the SiC–SiO_2 interface appear to be resilient to hydrogen

passivation at moderate temperatures [16-18], indicating that P_b centres are not the dominant defect type.

Conversely, a slight reduction in the density of rather deep states has been reported when the H_2 annealing temperature is increased beyond 700 ^{0}C [17, 18]. This slight improvement is considered to be a result of hydrogen passivated dangling carbon bonds (P_{bC}-type centres), implying that the origin of the high density of electrically active defects remaining throughout the SiC band gap cannot be ascribed to Si and C dangling bond type defects. The overall ineffectiveness of traditional hydrogen-based passivation techniques tends to provide a strong indication that the origin(s) of the dominant defects at SiC–SiO_2 interfaces are, in fact, very different to that observed at Si–SiO_2 interfaces and therefore, the SiC–SiO_2 interface requires alternative passivation techniques.

The most universally regarded hypothesis for the inferior electrical properties of as-oxidized SiC–SiO_2 MOS structures is the presence of carbon at the interface as a result of the complex oxidation kinetics of SiC [Eq. (4.1)], which leads to elemental carbon clustering and suboxide bonding at the interface [18], combined with the inherently wider bandgap of SiC, which encompasses a greater range of defects levels otherwise inactive in Si [12].

Physical studies have directly supported this hypothesis by revealing that a significant amount of residual carbon remains at the interface once the oxidation process is terminated in the form of a thin, carbon-rich transitional sub-oxide layer [19-22]. Presumably, this complex interfacial region comprises of carbon-based graphic-like and sp^2-bonded clusters at the interface and near-interfacial oxide defects bordering the interface that may appear electrically active in respect the SiC bandgap. The dominance of carbon based defects is further supported the reduction in D_{it} that is observed on SiC faces with a lower concentration of surface carbon atoms

[6, 18]. Using a variety of characterisation techniques on SiC MOS capacitors the defect sources that contribute to the extremely poor quality of as-oxidised SiC–SiO_2 interfaces have been systematically linked to specific energy levels, forming the widely accepted "carbon cluster model" [18, 23]. According to this model, shown in Fig. 4.1, a significant portion of interface trap spectrum in SiC MOS devices can be accounted for by the combined influence of π-bonded, sp^2-hybridized carbon atoms that are arranged in various sized clusters[24]. Small carbon clusters, that bear

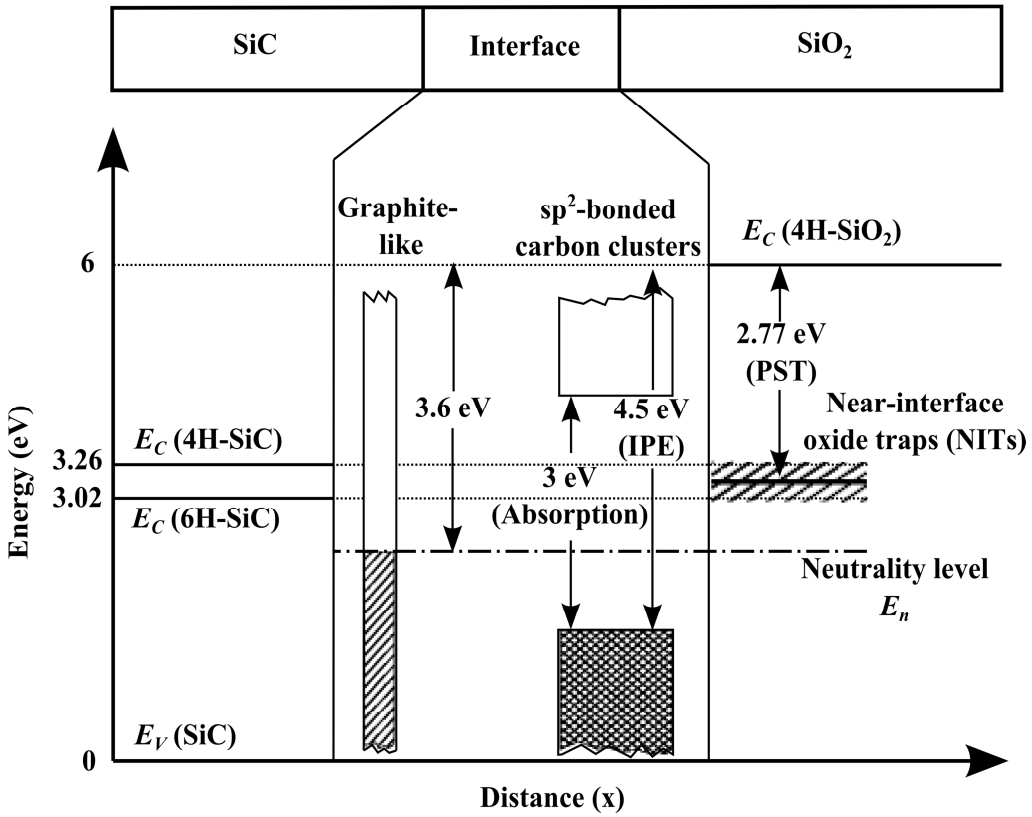

Figure 4.1 The proposed "Carbon cluster model" representing the origins of the electrically active defects in SiC–SiO_2 MOS structures investigated by internal photoemission (IPE), photon stimulated electron tunneling (PST) and absorption techniques. Defects located above the neutrality level (E_n) are predominantly considered to be acceptor-like with the remainder predominantly donor-like [18, 23].

resemblance to the electron states observed in wide band gap (3 eV) amorphous hydrogenated carbon (a-C:H), are considered to be responsible for the high D_{it} distributed in the lower half of the band gap observed in all common SiC polytypes (3C, 4H and 6H). These small clusters located above the SiC valance band exhibit donor-like behaviour, explaining the considerable positive charge observed in *P*-type SiC MOS structures. [18]. It has been demonstrated that these states can be significantly reduced by pre-oxidation cleaning of silicon carbide surfaces by ultraviolet radiation and oxygen [25]. This indicates that excess carbon at the SiC–SiO_2 interface also originates from intrinsic sources prior to oxidation.

As carbon accumulates at the SiC–SiO2 interface during oxidation, larger clusters with a gapless, graphite-like distribution of electron states are believed to form. The broad energy range of these clusters spans the entire SiC band gap which tends to account for the D_{it} continuum typically observed in SiC MOS capacitors. These graphite-like clusters are considered to be electrically amphoteric, and therefore, can exhibit both donor-like and acceptor-like trapping behaviour. The defect trapping behaviour is separated by a neutrality level (E_n) that is considered to be approximately equal to Fermi level position in graphite. Defects located above the neutrality level are predominantly considered to be acceptor-like with the remainder below E_n considered to be predominantly donor-like. Thus the occupancy and charge state of these defects depends on the position of the Fermi-level in the SiC relative to the neutrality level of the graphic-like clusters. Rigorous surface cleaning and oxidation loading procedures [5], combined with wet re-oxidation annealing [10] have shown to significantly reduce the D_{it} near the midgap to the low-10^{10} eV^{-1} cm^{-2} range. However, the channel-carrier mobility in 4H–SiC MOSFETs appeared to be unaffected by these improvements and remained in single digits.

While the existence of elemental carbon cluster type defects seem to provide a satisfactory explanation for the comparable D_{it} distribution in the lower half of the SiC band gap of common polytypes, they cannot adequately describe the dissimilar D_{it} distributions observed in the upper half of the SiC band gap. In as-oxidized 4H–SiC MOS devices, the D_{it} energetically located near the conduction band tends to exceed 10^{13} cm^{-2} eV^{-1}, which is considerably higher than the interface trap density observed over the remainder of the band gap [18, 26, 27]. As a possible explanation, the enhanced D_{it} observed in the upper half of the SiC band gap has been ascribed to the presence of near-interfacial oxide traps (NITs), exhibiting acceptor-type behaviour. Photon stimulated electron tunneling (PST) investigations, performed on MOS structures fabricated by oxidation of Si, 4H and 6H–SiC surfaces suggest that a narrow distribution of oxide-based defects are similarly concentrated around energy level approximately 2.8 eV below the conduction band of the SiO_2 in all substrates [28, 29]. These defects are considered to be particularly detrimental to the inversion channel-carrier mobility in 4H–SiC MOSFETs, given that their observed density is excessively high and their energy level almost coincides with the conduction band in 4H–SiC [2, 3, 18, 29]. While the exact atomic structure of these defects remains unclear, they are considered to be associated with oxygen vacancies which are formed during oxidation of both Si and SiC and most likely enhanced by the presence of carbon at the SiC–SiO_2 interface [30, 31].

In order to improve the performance of 4H–SiC MOSFETs, the excessive density of electrically active defects that dominate the electrical characteristics of the 4H–SiC/SiO_2 interface must be sufficiently reduced either by passivation techniques or their generation minimized during the oxidation process. Incorporating nitrogen at the SiC–SiO_2 interface by means of gate oxide nitridation, either through the direct growth or post oxidation annealing of standard oxides in a high temperature, nitrogen-

containing gas precursor such as nitric oxide (NO) or nitrous oxide (N_2O), has been heralded as one of the most effective techniques in reducing the D_{it} throughout the SiC bandgap, particularly near the 4H-SiC conduction band, whilst maintaining or improving the bulk properties of the oxide layer. This key technological breakthrough is responsible for the development of SiC–SiO_2 interfaces with acceptable electrically properties that have led to the commercial release of SiC based MOS devices in recent years. Given the immense importance of nitrogen at the SiC–SiO_2 interface in the development of device-grade SiC MOS structures the following section provides a brief overview on the process of gate oxide nitridation.

4.2.2 Defect Passivation: The Effects of Nitrogen at the SiC–SiO_2 Interface.

Li *et al*. [32] initially demonstrated that a high temperature (1100 ^{0}C) post oxidation anneal (POA) in nitric oxide (NO) significantly reduced the D_{it} at the 6H–SiC/SiO_2 interface. In following, Chung *et al.* [33] demonstrated that NO annealing significantly reduces the D_{it} throughout the bandgap in 4H–SiC MOS capacitors and was particularly effective in reducing the large density of NITs situated near the 4H–SiC conduction band. Subsequently, Chung *et al.* [9, 34] revealed that NO annealing of standard dry oxides enhances the channel-carrier mobility in 4H–SiC MOSFETs by approximately an order of magnitude (≈ 35 cm^2/Vs) and improved the turn-on characteristics by significantly reducing the threshold voltage. The enhanced channel-carrier mobility was related to roughly an eight-fold reduction in the density of NITs energetically positioned near the 4H–SiC conduction band edge as shown in Fig. 4.2. In addition, it was demonstrated that NO annealed oxides produce barrier heights close to theoretical values [35] and therefore, are less susceptible to electron injection mechanisms, enhancing the reliability of devices operated at high electric fields and temperatures. Similar improvements to the SiC–SiO2 interface and bulk

oxide properties have also been demonstrated by using nitrous oxide (N2O) as an alternative nitridation precursor [32, 36-38].

The beneficial effects of gate oxide nitridation by NO and N_2O on the electrical properties of SiC MOS devices has been attributed to nitrogen (N) bonding at the interface. Physical analysis by secondary ion mass

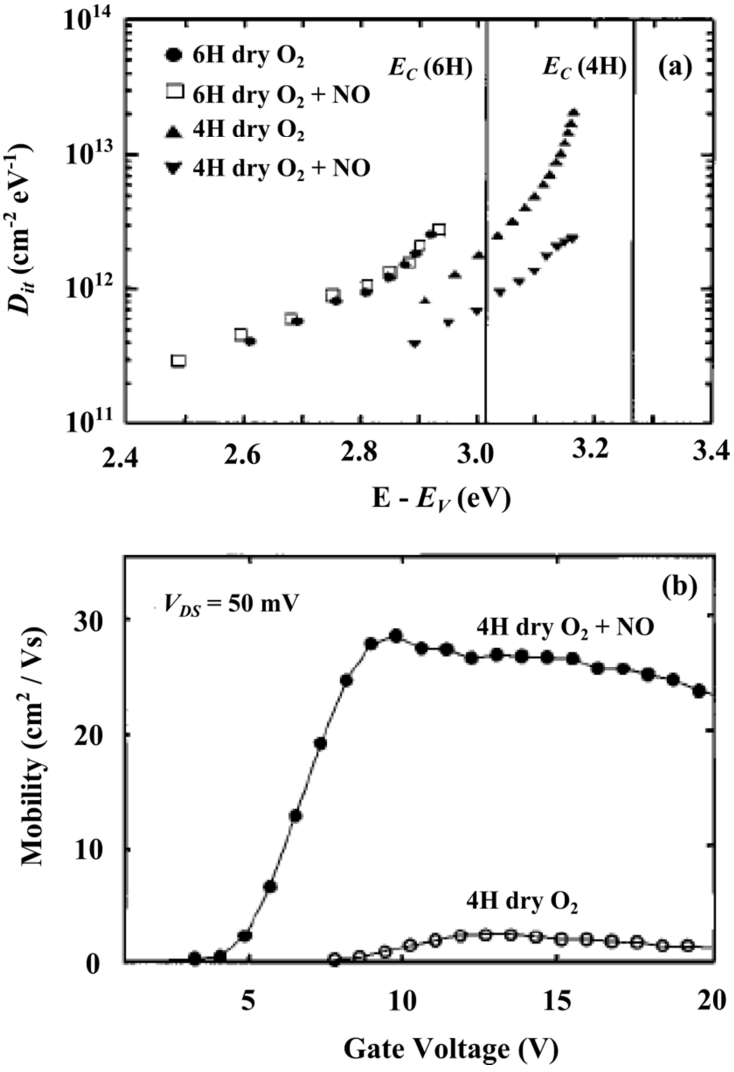

Figure 4.2 (a) Interface trap density acquired from high-low C–V and AC conductance measurements on 4H– and 6H–SiC MOS capacitors before and after post oxidation anneals in NO at 1175 ^{o}C for 2hr. (b) The corresponding 4H–SiC MOSFET channel-carrier mobility [9].

spectroscopy (SIMS) reveals that nitrogen is exclusively incorporated at $SiC–SiO_2$ interface, with distribution profile analogous to the $Si–SiO_2$ interface; however the nitrogen concentration is considerably lower [39]. Analysis of the N 1s core spectrum by X-ray photoelectron spectroscopy (XPS) reveals that the binding energy of the nitrogen peak at both interfaces is very similar to that of silicon nitride [40].

According to *nitridation model* proposed by Jamet *et al.*[41], the electrically active defects at the $SiC–SiO_2$ interface are reduced by nitridation as a result of two main mechanisms: (1) the passivation of dangling and strained bonds by the formation of strong Si≡N bonds, and (2) the removal of carbon and associated silicon–oxycarbon complexes from the interfacial region. Evidence of the former process has been demonstrated by comparing the XPS Si 2p spectrum at the $4H–SiC/SiO_2$ interface of dry oxides annealed in argon, NO or N_2O [42]. The interfacial region of the gate oxide annealed in argon is broader and more complex than the oxides annealed in either NO or N_2O as shown in Fig 4.3. This implies that gate oxide nitridation provides a more orderly interface by effectively diminishing a number of sub-oxide bonding arrangements and reducing the intensity of the carbon based bonding arrangements that remain.

It has been proposed that the reduction of interfacial carbon related defects is associated with the existence of C–N bonding at the $SiC–SiO_2$ interface, that has been observed by numerous groups following nitridation of the gate oxide [33, 41, 43]. Afanasev *et al.* [44] suggests that C–N bonding effectively passivates carbon related defects remaining at the interface, rendering them electrically inactive, as well as providing an additional out diffusion pathway for accumulated carbon in the form of a compact CN molecule. Both of these mechanisms could account for the reduced interface trap density as a result of gate oxide nitridation.

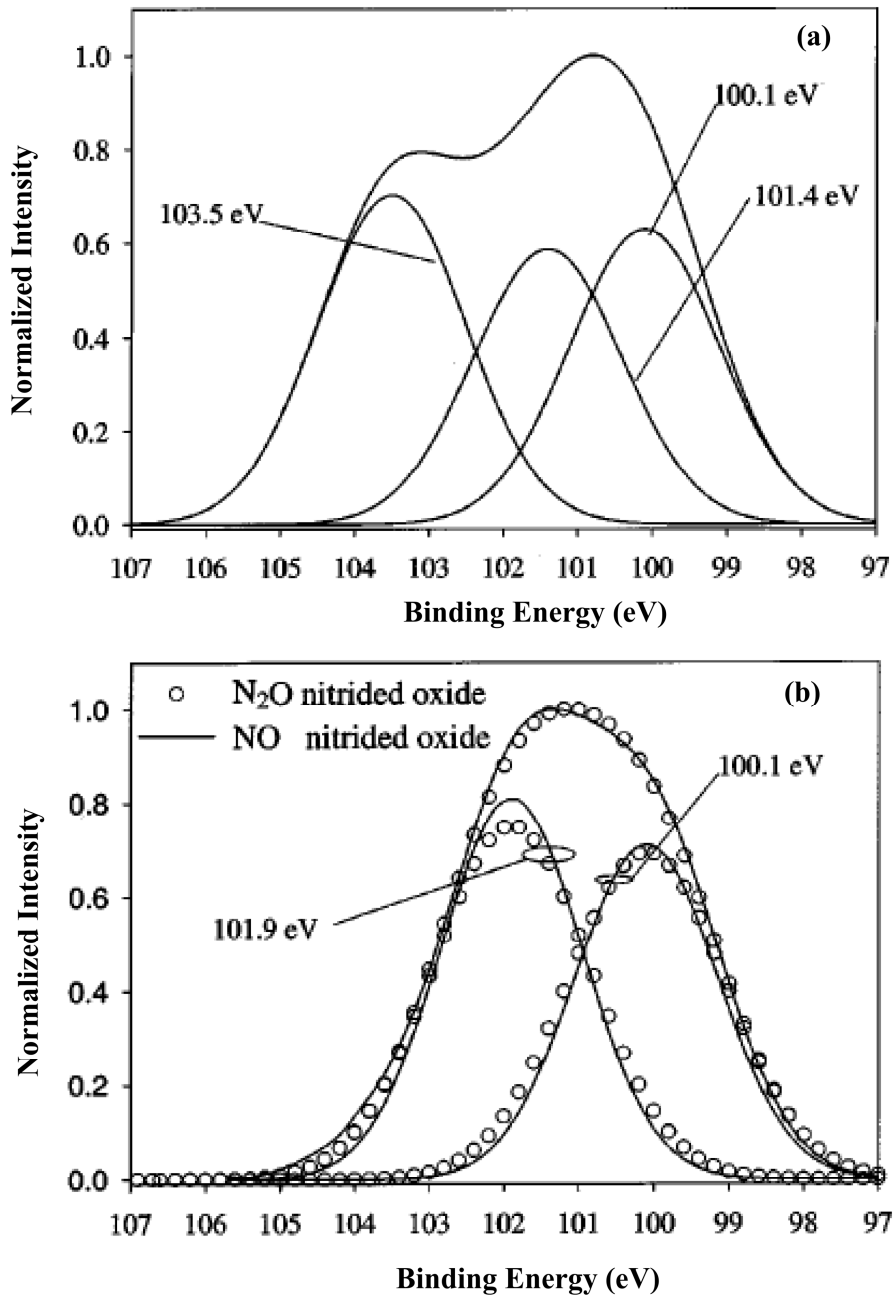

Figure 4.3 (a) Si 2p XPS spectrum at the argon annealed 4H–SiC/SiO_2 interface. (b) Si 2p XPS spectrum at the NO and N_2O annealed 4H–SiC/SiO_2 [42].

Another key observation, obtained from Z-contrast imaging and electron energy loss spectroscopy conducted by Biggerstaff *et al.*[21], is the reduction of the transitional Si-O-C layer width as a result of NO annealing.

In the same study, Biggerstaff *et al.*[21] also found the width of the transition layer to be inversely proportional to the effective channel mobility measured on fabricated devices. The reduction of the transitional layer thickness seems to provide a feasible physical explanation as to why gate oxide nitridation is particularly efficient in reducing the NITs in the upper part of the 4H-SiC band gap.

As the mechanisms of nitridation has been related to various bonding arrangements of nitrogen at the interface the resulting effects of gate oxide nitridation on the electrical properties of the SiC–SiO_2 interface has shown a strong correlation to the amount of nitrogen incorporated at the interface. Consequently the main objective in the development of gate oxide nitridation processes is to maximize the amount of nitrogen incorporated at the SiC–SiO_2 interface.

According to both SIMS and XPS analysis the nitrogen peak intensity at SiC–SiO_2 interface following nitridation by annealing or direct growth in NO at 1150 °C is slightly high than equivalent processes carried out in an N_2O ambient [42]. Calculation of the atomic percentage of nitrogen at the interface from the XPS spectra reveals that approximately 1.4 at. % of nitrogen is incorporated at the SiC–SiO_2 interfaces annealed or directly grown in NO compared to approximately 1.2 at. % for the case of SiC–SiO_2 interfaces annealed or grown in N_2O. A similar tendency was also observed by nuclear reaction analysis, where the atomic concentration of nitrogen at the NO-annealed SiC–SiO_2 interface was found to be an order of magnitude higher than at the N_2O-annealed interface [45]. It has been considered that the complex decomposition of N_2O, which results in two competing processes: (1) defect formation due to the oxidation of the SiC surface by O_2 and (2) defect passivation/removal by nitrogen due to the decomposition of NO, is responsible for the reduced accumulation of nitrogen at the SiC–SiO_2 interface in comparison to pure NO [42]. Whist the N_2O nitridation

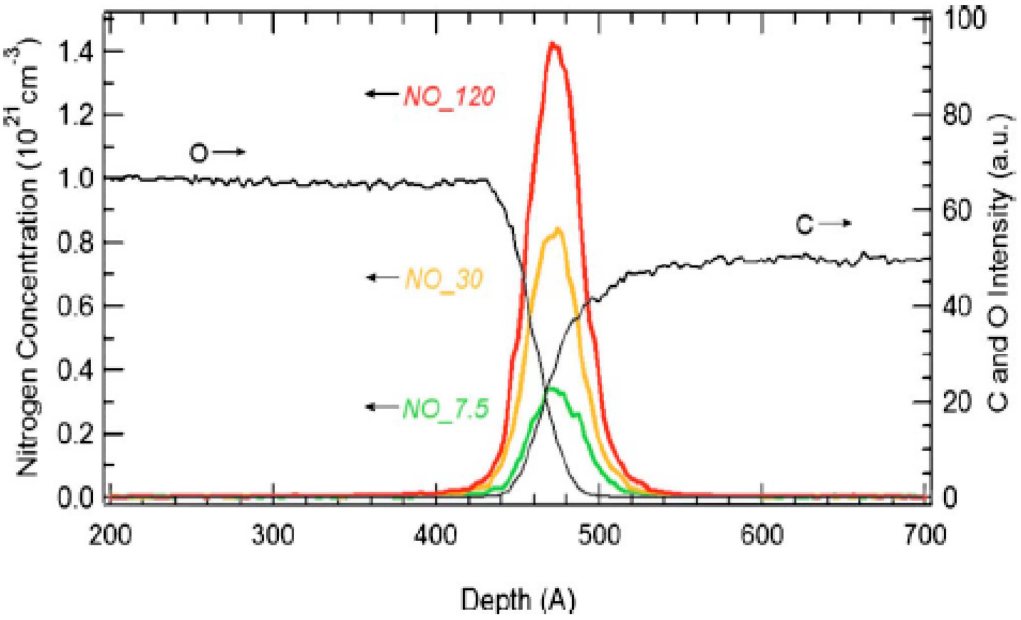

Figure 4.4 SIMS profiles of the nitrogen incorporated at SiC–SiO_2 interface following anneals in NO at 1175°C for 7.5, 30, and 120 mins [46, 47].

precursor gas is less effective than NO it is however non-toxic, and thus preferred in industry.

For a given temperature and gas-flow rate it has been demonstrated through SIMS analysis that the amount of nitrogen content incorporated at the as-oxidized SiC–SiO_2 interface progressively increases as a function of the NO annealing time (Fig. 4.4) [46, 47]. As demonstrated by Rozen *et. al* in Fig. 4.5 [46, 48], this incremental accumulation of nitrogen at the interface as a function of NO annealing time directly corresponds to a progressive reduction in the D_{it} throughout the 4H–SiC bandgap, particularly near the conduction band, and progressively enhances the transfer characteristics and the resulting channel-carrier mobility in 4H–SiC MOSFETs. While these results clearly illustrate the positive effects of NO nitridation in improving the electrical properties of the SiC–SiO_2 interfacial

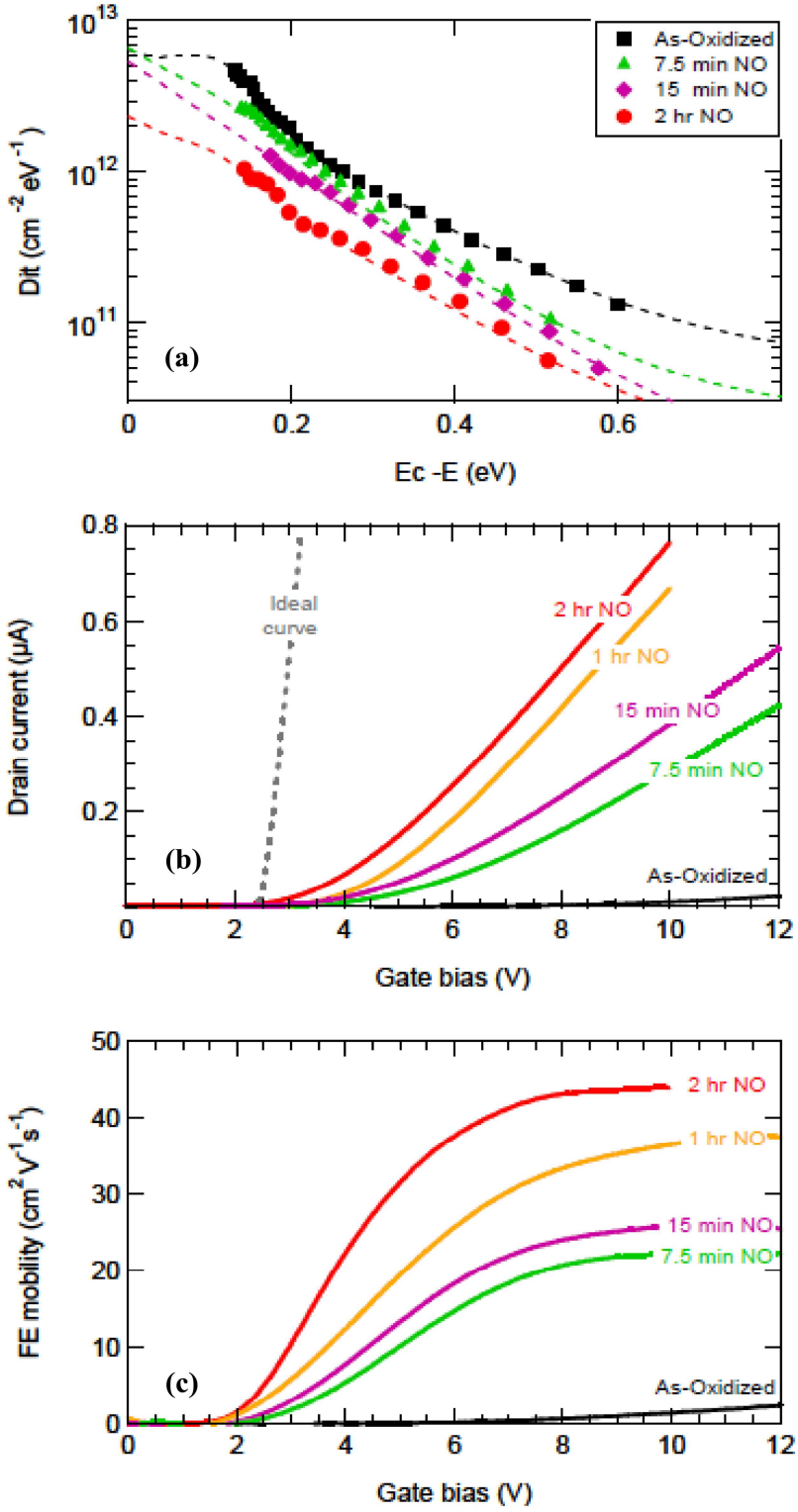

Figure 4.5 Corresponding interface trap densities (a), transfer characteristics (b), and field-effect mobilities (c) observed in 4H–SiC MOS devices as a function of NO annealing time [46, 48].

region the effect saturates, and the channel-carrier mobility remains considerably lower than that in the SiC bulk.

It has been observed that the amount of nitrogen incorporated at the SiC–SiO_2 interface typically saturates at an areal density of around ~10^{14} cm^{-2} [45, 49]. According to McDonald *et. al* [49], the passivation of electrically active defects only depends on the nitrogen content and not the NO anneal time or temperature. The example given in their study demonstrating that NO annealing at either 1050 °C for 2 hrs or 1100 °C for 0.5 hrs produces a similar nitrogen content of ~2.4×10^{14} cm^{-2} and corresponds to similar interface trap densities observed throughout the SiC bandgap. In contrast, Rozen *et al.* [46-48] report that the accumulation of nitrogen and corresponding improvements of the SiC–SiO_2 interface saturates at an NO annealing time of ~2 hrs at 1175 °C. Given the limited experimental details it can only be speculated that high annealing temperatures (> 1100 °C) seem to affect the interfacial nitrogen content. In both cases, the amount of nitrogen incorporated at the interface is believed to be governed by the slow re-oxidation process that occurs simultaneously with the nitridation mechanisms, due to the O_2 formed from the NO decomposition process [50]. Once these reactions reach equilibrium the oxide thickness increases and the nitrogen content is considered to saturate [51].

Contrary to POAs in NO, thermal oxides directly grown in pure NO (oxynitridation) at high temperature on both 4H–SiC [41, 42] and 6H–SiC [52] have shown to exhibit the best SiC–SiO_2 interfacial qualities. These improvements are considered to be an effect of the nitridation-based carbon removal mechanism that begins at the initial oxidation phase of the SiC surface and continues simultaneously with the carbon accumulation/release process at the interface during the consumption of SiC throughout the oxynitride growth process, until it is terminated [41]. Thus the formation of electrically active, complex carbon based compounds and carbon clustering

is minimized during the growth process due to the beneficial effects of nitridation. However the kinetics of NO-oxynitridation is extremely slow. A 6 hr process at a temperature of ~1150C in a pure NO environment typically yields an oxide thickness of ~15 nm, which is equivalent to a growth rate of only ~2.5 nm/hr [42]. While the exceptionally retarded growth rate may allow sufficient time to maximize the benefits of the nitridation mechanisms and relieve strained chemical bonds, the major disadvantage of NO-oxynitridation is the impracticality of growing thick oxides required for power MOS devices.

Among several practical approaches to further improve the gate oxide process beyond that achieved by NO annealing, Cheong *et al.* [53] observed additional improvements of the SiC–SiO_2 interface by introducing an initial NO-nitridation process prior to oxidation and NO annealing, therefore implementing a *sandwich* (nitridation–oxidation–nitridation) type process using 100 % NO nitridation steps. Based on the evaluation of the HF etched-back SiC–SiO_2 interface roughness by atomic force microscope scans, Cheong *et al.* [53] concluded that the initial nitridation process played a key role in avoiding the formation of pronounced *oxide islands* prior to the very beginning of the main oxide growth. Schorner *et al.* [54] reported a promising low field mobility of 48 cm^2/ Vs together with a threshold voltage of 0.6 V for lateral enhancement-mode MOSFETs by adopting a similar *sandwich* gate oxide growth process.

4.3 NITRIDATION OF 4H–SIC GATE OXIDES AT LOW PARTIAL-PRESSURE: SIGNIFICANTLY REDUCING THE CONSUMPTION OF NITRIC OXIDE

Having discussed the thermal oxidation of SiC there is substantial evidence in reviewed literature that the high density of electrically active defects in SiC–SiO_2 MOS structures originates from elemental carbon clustering at the

interface and a thin, carbon-rich, transitional sub-oxide layer. Both of which are inevitably formed during standard dry and wet oxidation of the SiC surface due to the complex oxidation kinetics that entails the release of carbon.

The most effective process in reducing the D_{it} throughout the SiC bandgap and particularly, the high density of NITs near the 4H–SiC conduction band, has been gate oxide nitridation. This process relies on the decomposition of NO to incorporate atomic nitrogen at the SiC–SiO_2 interface, where the amount of nitrogen accumulated at the SiC–SiO_2 has been correlated to the improvement in the electrical characteristics of SiC MOS devices.

High temperature post oxidation annealing in pure NO is the most common method of nitriding the SiC–SiO_2 interface to fabricate device-grade oxide layers. Additional benefits have been obtained by implementing a *sandwich* (nitridation–oxidation–nitridation) type process using 100% NO nitridation steps. These results combined with the improvements associated with direct oxide growth in NO tend to suggest that the presence of NO throughout the oxidation process may be required to further enhance the properties of SiC–SiO_2 interfaces. However, due to low oxide growth rates, toxicity, and the expense of NO gas, this tends to limit the practicality of developing nitridation processes in pure NO or mixtures containing high partial-pressures of NO to small scale research-type oxidation furnaces due to the sheer volume of gas required. A majority of the nitridation processes in the literature report the use of 100% NO although little is known about the effects of NO nitridation on SiC MOS structures at low partial pressures which may be beneficial for larger oxidation furnaces given the ever increasing size of 4H–SiC wafers.

In this section, a series of gate oxides grown in O_2 and nitrided/grown in NO at very low-partial-pressures in a large scale oxidation furnace, representative of an 8-inch diameter production based model, to limit the consumption of NO are investigated by evaluating the electrical characteristics of *N*-type, 4H–SiC MOS capacitors. To integrate the benefits of NO-nitridation throughout the gate oxide growth process whist maintaining an acceptable growth rate a novel, combined oxidation-nitridation process at low partial-pressure is presented.

4.3.1 Experimental Details

Sample Preparation

The MOS capacitors used in this experimental analysis were fabricated on Si-faced, N-type 4H–SiC substrates, orientated 8° off-axis to the (0001) plane with a 10 µm epitaxial layer, doped by nitrogen to a concentration of 10^{16} cm^{-3}. These substrates were purchased from CREE Research Inc. (USA). Prior to oxidation, the samples were first rinsed in acetone and isopropanol followed by deionised (DI) water. This was followed by a piranha etch consisting of sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) at a ratio of 4:1 at 90°C for 15 minutes to remove any remaining traces of photoresist or any other organic residues. The samples then underwent further wet chemical cleaning by following the Radio Corporation of America (RCA) standard cleaning procedure to remove any remaining traces of organic, ionic and particulate contaminants. Between each RCA cleaning step the samples were thoroughly rinsed by immersion in running DI water for 5 minutes. Immediately prior to oxide the samples were placed in a 10% hydrofluoric (HF) solution for 1 minute to remove any native oxides and subsequently dried using pressurized nitrogen.

MOS Capacitor Fabrication Procedures

All gate oxides were grown in a resistively heated, horizontal SiC tube furnace displacing 37 L that is representative of an 8-inch diameter

production based model. The volumetric gas flow rate was kept at 5 standard litres per minute (SLPM) at all times to ensure a viscous gas flow of 0.08 m/s. This flow rate was experimentally determined for sufficient safeguarding against external ambient back-streaming and process control. Samples were loaded into the furnace at an idle temperature of 350 °C. An initial nitrogen purge out step was performed for 5 hours prior to temperature ramping to ensure an inert ambient for avoidance of low temperature oxide growth. The temperature was ramped at a rate of 5 °C/min with 20 minute stabilization steps at both 800 °C and 1000 °C.

Gate oxides were grown at 1250 °C by a variation of three different oxidation procedures at low partial pressures. The low partial pressures were achieved by buffering the precursor gasses with inexpensive, ultra-high purity nitrogen. The growth rate of the bulk oxide growth phase, common to all samples, was decoupled from the high temperature oxidation rate by reducing the partial-pressure of the O_2 to 5 %. The partial-pressure of NO was restricted to a mere 2 % where required to significantly reduce the consumption of the gas. For comparison, three sets of gate oxides were grown. The control sample was grown in dry O_2 (labelled O_2) for 9 hours as a base reference. A second, *sandwich* type process (labelled $NO/O_2/NO$) consisted of a pre-oxidation anneal in NO for an hour, followed by bulk oxide growth in dry O_2, for 9 hours, and finalised with a NO post oxidation anneal for an hour. The final oxidation process consisted of growth in NO and dry O_2 (labelled $NO+O_2$) combined gas ambient for 9 hours. After the oxidation and nitration phases the furnace was purged with nitrogen for 40 minutes to exhaust any remaining active gasses and subsequently cooled back down to idle temperature at a rate of approximately 5 °C/min. Detailed graphical representations of these processes are shown in Fig. 4.6.

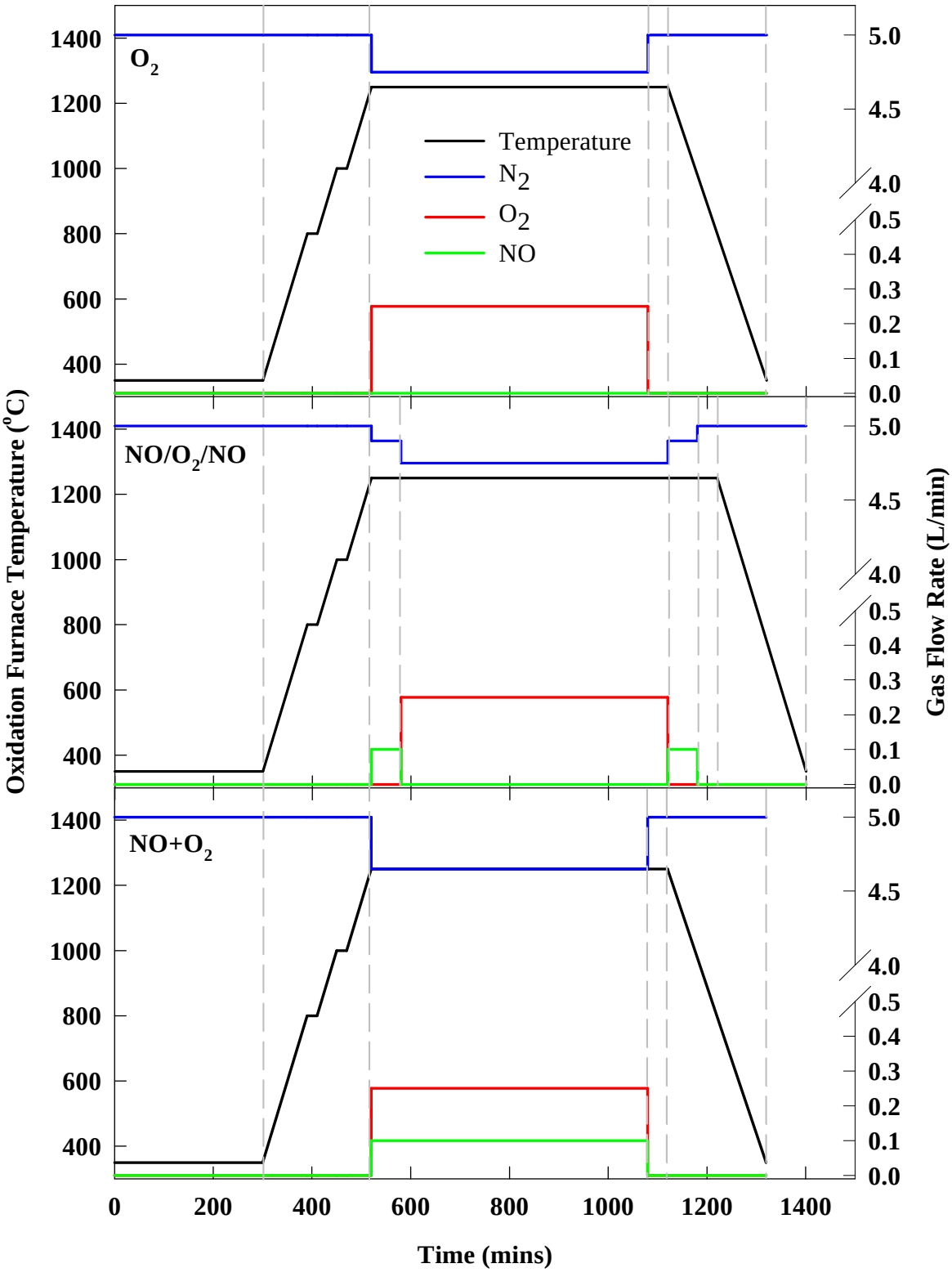

Figure 4.6 Detailed graphical representation of the low-partial pressure oxidation processes. The grey broken lines represent the oxidation process steps as explained in the text.

Directly after unloading, 300 nm thick Aluminium was sputter deposited on the oxide and defined by photolithography to form square gate contacts with an area of 0.0025 cm^2. To complete the MOS capacitor fabrication process the native oxide on the N^+ substrate was removed with 10 % hydrofluoric acid followed by aluminium deposition to form a large area ohmic contact.

Electrical Characterization Procedures

High-frequency capacitance-voltage (C–V) and conductance-voltage (G–V) measurements were obtained by sweeping the MOS capacitors between strong accumulation and deep depletion by applying gate biases of ± 10 V. The superimposed AC signal amplitude was equal to 50 mV. A slow sweep rate of 0.1V/s was applied to allow equilibrium between the trap states and the DC component.

Measurements were acquired for a range of frequencies between 1 kHz and 100 kHz to characterise an array of corresponding interfacial trap response times. Gate oxide thicknesses were determined by measuring the oxide capacitance at 100 kHz with the capacitor biased well into accumulation. The flat-band voltages were extracted by matching the flat-band capacitance corresponding to the V_{FB} of the ideal C-V curve which was calculated using an analytical computer program based on the approaches described by Schroder [55]. The effective interface trapped charge (Q_{it}) was determined by the frequency dispersion of the flatband-voltage (ΔV_{FB}) between the 1 kHz and 100 kHz *C–V* curves by

$$Q_{it} = \frac{C_{ox}\,\Delta V_{FB(1-100\,kHz)}}{qA} \tag{4.1}$$

where A defines the gate area, q the electric charge and C_{ox} the oxide capacitance measured in strong accumulation.

Interfacial qualities were accessed by the analysis of Q_{it} as well as the near-interface trap profile in terms of density and spatial distribution according to the theory described in Chapter 3. These profiles were extracted from the accumulation conductances obtained from the G–V curves for gate biases corresponding to a moderate oxide electric field strength of 1.5 MV/cm in order to avoid any discrepancies from oxide thickness variations. Current-voltage (I–V) characteristics were obtained by positively steeping the gate voltage in 200 mV increments to induce electron injection from the conduction band of the SiC into the gate oxide. Knowing the area of the gate electrode and the oxide thickness, the current-voltage data was converted into a current density vs electric field plots. From these plots the oxide integrity was assessed by the extraction of the SiO_2/SiC conduction band offset barrier heights by employing Fowler–Nordheim analysis. All measurements were performed using an Agilent B1505A power device analyser/curve tracer in a light and electrically shielded probing station at a control temperature of 25°C.

4.3.2 Results and Discussion

Evaluating the SiC–SiO_2 Interface

Figure 4.7 illustates the high-frequency C–V and G–V curves of the various N-type 4H-SiC MOS capacitors swept from strong accumulation to depletion at frequencies between 1 kHz and 100 kHz. The G–V curves are plotted separately to improve clarity and resolution. From the C–V curves, it can easily be seen that frequency dispersion is significantly reduced for both processes containing NO in comparison to the O_2 only process. In accordance with the conventional MOS interface characterisation techniques outlined in Chapter 2, this frequency dispersion implies that the interface states are only partially responding to the measurement signal frequency, where the corresponding electron emission rates of these states are within the measurement frequency range of the AC signal. At higher

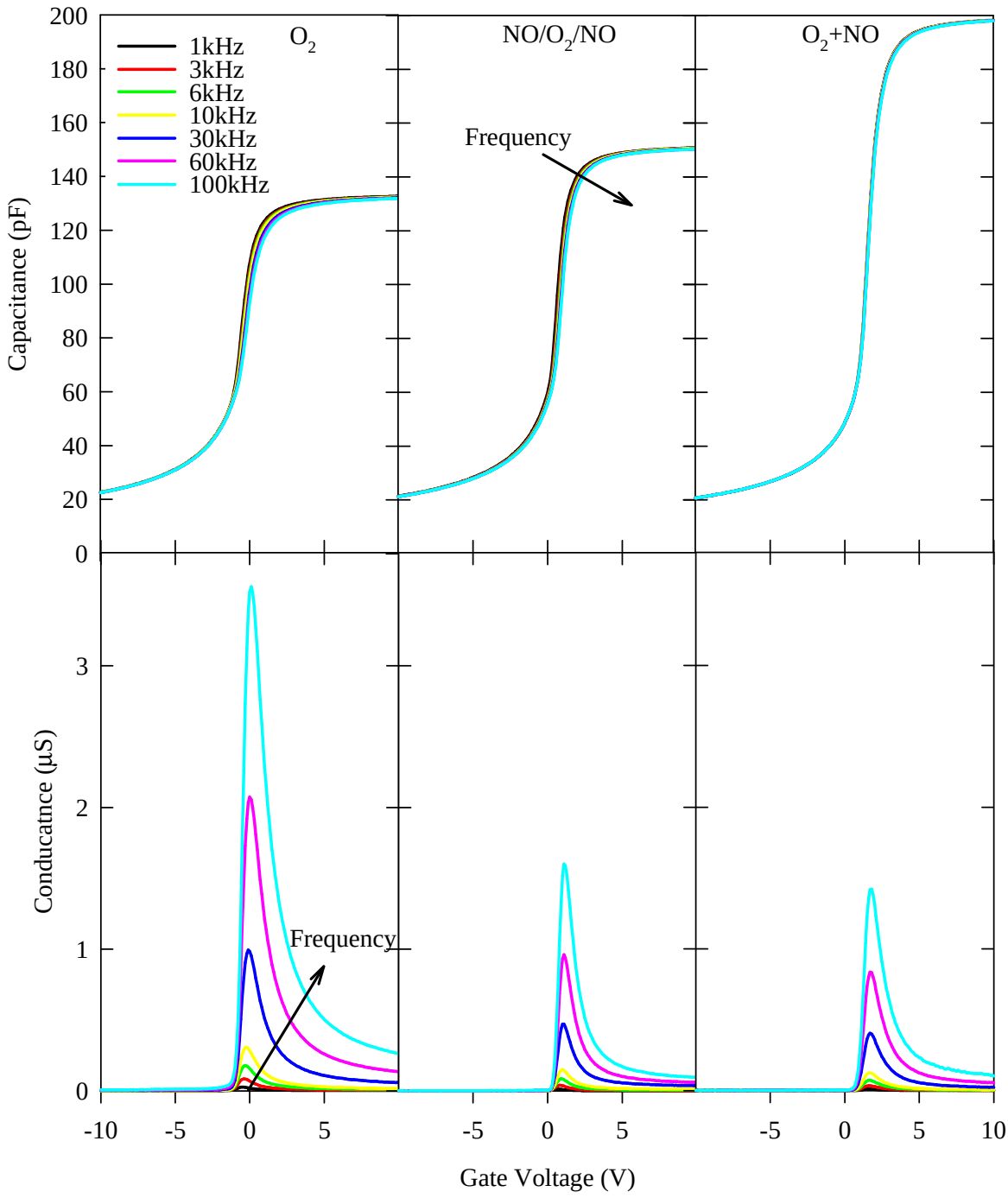

Figure 4.7 High–frequency capacitance–voltage (C–V) and conductance–voltage (G–V) measurements for N-type 4H-SiC MOS capacitors corresponding to the three different low-partial-pressure oxidation processes. Trends due to the increasing measurement frequency are indicated by the arrows.

frequencies fewer states can respond to the measurement signal and therefore, are consequently filled with electrons, effectively inducing negative charge that results in a shift or stretch-out of the C–V curve toward positive gate biases. At lower frequency a larger portion of states are able to follow the measurement signal which results in less charge trapping and accordingly, less C–V stretch-out along the gate bias axis. The frequency dispersion corresponding to the shift in flat-band voltage provides an indication of the interface trap density energetically aligned to the SiC energy band, near the conduction band edge, as the MOS capacitor borders the accumulation region of operation. Interface states located near the conduction band edge have been the main focus of previous studies based on electrical measurements SiC MOS capacitors [29, 56]. The 4H-SiC polytype in particular has shown a strong dependence between the location of these traps and the inversion channel mobility as presented in numerous literature reports[9, 33, 57]. These shallow states are apparently responsible for severe trapping of mobile carriers causing significant reduction in the effective channel mobility [27, 58].

From the shift associated with the flat-band voltage the amount of charge trapped in these states can be quantified and compared using Eq. (4.1). The effective interface trap charge (Q_{it}) as well as the oxide thickness (t_{ox}), flat-band voltage (V_{FB}) and the flat-band voltage shift (ΔV_{FB}) extracted from the high-frequency C–V curves are summarized in Table 4.1. From these results several key observations can be made.

First and foremost, both processes involving NO at low partial-pressure exhibit less C–V curve frequency dispersion in contrast to the dry O_2 reference process. This corresponds to a noticeable reduction in the ΔV_{FB} and consequently, the calculated Q_{it}. Surprisingly, the combined process that has a considerable amount of O_2 throughout the oxidation/nitridation process, in comparison to the final NO anneal of the sandwich process,

shows the greatest improvement of the SiC/SiO_2 interface by the suppression of the interface states aligned to the 4H-SiC band gap. This reduction of interface states is also evident through the reduction of the measured conductance peak values that are situated at gate biases corresponding to the MOS capacitor in depletion mode. All conductance measurements presented in Fig. 4.7 exhibit substantial asymmetry of the peak towards the accumulation regime. They also reveal noticeable measured conductance at gate biases corresponding to accumulation. These traits tend to be typical for SiC MOS structures presented in the literature [29, 59, 60].

Conventional MOS interface theory suggests that these effects are a result of parasitic series resistances, principally arising from the substrate contact and measurement probes, based on the equivalent circuits

TABLE 4.2. Comparison of electrical parameters extracted from high-frequency C–V measurements. or aligned to the conduction band, which would correspond to degenerate conditions and the measured conductance observed on 4H-SiC MOS capacitors biased well into accumulation.

Parameter	Unit	Oxidation Process		
		O_2	$NO/O_2/NO$	$NO+O_2$
t_{ox}	nm	65.1	57.0	43.3
$V_{FB\ (1\ kHz)}$	V	0.16	1.16	2.08
$\Delta V_{FB\ (1\ kHz\ -\ 100\ kHz)}$	V	0.48	0.35	0.07
Q_{it}	$\times 10^{11}$ cm^{-2}	1.58	1.31	0.35

predicted by Lehovec's expressions [61]. However, as previously outlined in Chapter 3, this assumption seems to be a result of the classical trap-carrier transportation mechanism which is based on thermal emission as described by Shockley-Read-Hall theory for non-degenerate semiconductors biased to depletion. This theory cannot be applied to states in very close proximity to the conduction band.

Essentially, the trap response time given by SRH theory is exponentially dependant on the trap energy level in respect to the conduction band. The SRH theory therefore predicts that these particular states would respond virtually immediately and should not contribute to the MOS admittance under realistic measurement conditions. As outlined in Chapter 3, quantum confinement effects are pronounced in the MOSFET channel due to the very high electrical fields induced under strong inversion conditions and should be considered. Therefore, the channel electrons will be confined to two-dimensional energy subbands aligned to the conduction band. Consequently, additional band-bending will occur in an N-channel MOSFET under strong inversion biases, which will set the Fermi level well above E_C. Channel electrons from the inversion layer will therefore be able to communicate with near-interface oxide traps energetically aligned to the conduction band through quantum mechanical tunneling. These effects are also expected on N-type MOS capacitors biased well into accumulation due to the distinct similarities between the band structure and carrier type. It is the energetic position of these near-interface traps that are of particular importance in determining channel mobility as they become electrically active and trap a majority of the mobile channel electrons resulting in the significant reduction of the transconductance typically measured on 4H–SiC MOSFETs under gate biases corresponding to strong inversion.

To characterise the near-interface traps aligned to the conduction band the accumulation conductance, corresponding to a moderate oxide

electric field (E_{ox}) of 1.5 MV/cm was extracted and compared as a function of frequency in Fig. 4.8. The accumulation conductance was extracted a fixed E_{ox} to avoid any discrepancies that could possibly result due to oxide thickness variations. The electric field was simply determined by:

$$E_{ox} = \frac{V_G - V_{FB}}{t_{ox}} \tag{4.2}$$

where t_{ox} is the calculated oxide thickness from the measured oxide capacitance in accumulation, V_G the gate voltage and V_{FB}, the theoretical flat-band voltage of 4H-SiC. In this case, the ideal flat band voltage for *N*-type 4H–SiC corresponds to the metal (aluminium)–semiconductor work function difference which is equal to 0.27 V. The surface potential is considered negligible in strong accumulation and therefore can be omitted from the electric field calculation.

From the logarithmic plots presented in Fig. 4.8, it is clear that both oxidation processes containing NO exhibit lower accumulation conductance values over the range of measurement frequencies analysed. This implies that NO has effectively reduced the density of near-interface traps aligned to the conduction-band and according to the underlying theory developed in Chapter 3, should therefore correspond to an improvement in the effective inversion channel mobility of 4H-SiC MOSFETs. The enhancements of the 4H-SiC/SiO_2 interface as implied by reduction of the accumulation conductance are consistent with the well-known improvements of the interfacial properties and corresponding improvements in MOSFET mobility figures by NO that are commonly reported in the literature.

Moreover, these results also indicate that the conductance measured in accumulation is process dependent. Considering that all the MOS capacitors were fabricated from the same wafer, under identical fabrication

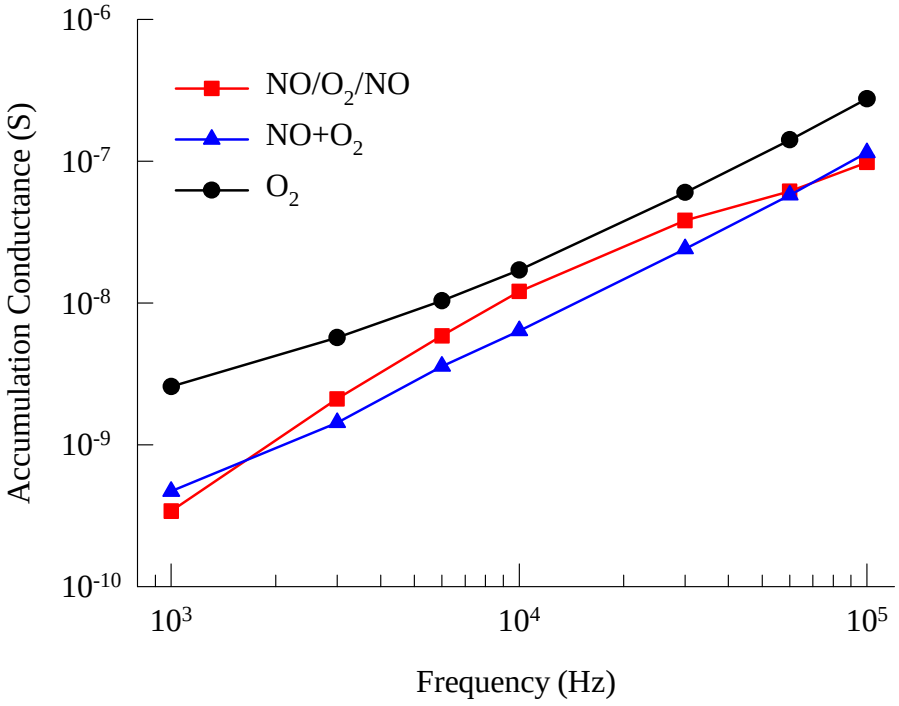

Figure 4.8 Semi-logarithmic accumulation conductance–frequency plots of 4H–SiC N-type MOS capacitors measured at a nominal oxide field of 1.5 MV/cm.

processes and measured using the same equipment in close succession, these results further justifies the hypothesis that the accumulation conductance observed on 4H–SiC N-type MOS capacitors is, in fact, a consequence of conduction band carrier-trap communication and not a direct result of parasitic series resistance effects as suggested by conventional interface theory.

The reduction of near-interface traps aligned to the conduction band, due to the beneficial effects of NO, also corresponds to the reduction of traps aligned to the 4H–SiC band gap, near the conduction band, as observed by the frequency dispersion of the *C*–*V* curves shown in Fig. 4.7. Evidently, this correlation may help to explain the rather apparent

relationship between the channel mobility of 4H-SiC MOSFETs and the D_{it} near the conduction band that is generally observed.

Figure 4.8 demonstrates that the accumulation conductance as a function of frequency is distinctly dependent on the gate oxidation process. Firstly, all accumulation conductance plots increase with measurement frequency. By applying the basic concepts of both the conductance method and tunneling model this dependence infers that the density of near-interface traps increases spatially towards the SiC surface. Between the measurement frequencies of 3 kHz and 60 kHz the NO/O_2/NO sandwich process exhibits higher conductance than the combined NO+O_2 process. This tends to imply that there seems to be a larger density of near-interface defects spatially localized away from the interface at distances directly related to the range of measurement signal period times in question. The most likely explanation for this observation is that the post anneal in only 2 % NO for one hour is simply insufficient to suppress the large number of active interfacial states stemming from the transitional carbon-rich layer that is formed during the thermal oxidation of the SiC substrate in dry O_2 [18, 25]. While these NITs seem to be somewhat resilient to the effects of the pre and post anneals in 2 % NO they appear to be suppressed by the simultaneous oxidation-nitridation processes occurring in the mixed ambient of 2 % NO + 5 % O_2. This is clearly indicated by the similarities observed between the accumulation conductance frequency trends of the O_2 reference and the NO+O_2 combined processes. Essentially, the combined process reveals a parallel reduction in the near-interface trap density corresponding to the range of measurement frequencies investigated.

These results suggest that the oxide growth kinetics between a standard thermal oxide formed under dry O_2 and subsequently annealed by NO nitridation are noticeably different than that of an oxide formed in a mixed ambient of NO and O_2. Gate oxides grown in pure NO are considered to exhibit the best interfacial properties [41, 52] in comparison to standard

thermal oxides annealed in NO; however the process is notoriously slow and therefore not suitable for the growth of sufficiently thick gate oxides. The extremely slow growth rate is typically attributed to the rather small amount of O_2 and subsequent growth of SiO_2 as a result of the disassociation of the NO molecules as well as the passivation effects of atomic nitrogen that are indicated by the pile up of N and the reduction of carbon based complexes at the SiC–SiO_2 interface region through physical studies [39, 42]. Interestingly, the addition of NO at low partial pressure throughout an otherwise standard dry O_2 process still significantly retards the growth rate, even though the dissociation of NO at the SiC–SiO_2 interface technically supplies additional oxygen.

The results in Table 1 indicate a substantial 50% reduction in the overall oxide thickness due to growth in a mixed low partial pressure NO+O_2 ambient. In addition, the sandwich process also exhibits a reduction in the oxide growth rate of around 14 %. This reduction has to be attributed to the effects of NO during the pre-annealing phase, prior to the bulk oxide growth in 5% O_2. In this case the initial oxidation rate due to the supplied O_2 must almost certainly be limited by the passivation effects associated with the initial formation of an N rich layer, mainly comprised of silicon-oxynitrides such as Si-O-N and strongly bonded Si≡N molecules[42]. This layer must impede the diffusion and reaction rate of oxygen and subsequent creation of SiO_2 from the bulk SiC. Once this layer is effectively diffused and penetrated the oxidation rate of the SiC that corresponds to the temperature and O_2 partial pressure resumes.

The formation or partial formation of a nitrogen rich layer as a result of atomic nitrogen bonding arrangements would also play a considerable role in the oxidation mechanisms of the combined NO+O_2 process. This would result in competing nitridation and oxidation processes throughout the newly evolving SiC–SiO_2 interface and therefore substantially limit the

overall gate oxide growth rate. The further improvements of the interfacial region during these competing processes can therefore be attributed to the simultaneous removal of carbon and associated complex silicon–oxycarbon bonds from the interface due to the incorporation of nitrogen originating from the NO nitridation process [37, 42]. In comparison, the POA in NO of the sandwich process has to contend with the removal of bulk carbon based and associated defects accumulated from the prior standard dry O_2 oxidation process.

The flat-band voltages extracted from the C–V curves and summarized in Table 4.1 also reveal considerable process induced variations, which may provide further insight into the properties of the SiC–SiO_2 interface. At low frequencies a large portion of interface states can respond to the measurement signal and therefore will have a lesser influence on the flat-band voltage. The V_{FB} corresponding to the O_2 reference process at 1 kHz is very close to the ideal however, the influence of interfacial states make this observation less than straight forward. The significant stretch-out of the C–V curves toward positive biases at higher frequencies indicates the presence of acceptor type states that become filled with electrons and consequently, resemble negative charge. In all likelihood the occurrence of similar acceptor type states, located deep in the SiC bandgap, can also be expected. The rather slow response time of these traps will make them undetectable to even the lowest of measurement frequencies (e.g. quasi-static conditions) and therefore they will behave like fixed negative charges. This implies that apparent near ideal V_{FB} value is a result of strong compensation effects occurring from the near-equal presence of fixed positive oxide charges.

In comparison, all processes involving the use of NO demonstrate positive flat-band voltage shifts compared to that of the dry O_2 reference. This positive shift can be interpreted as a net increase in negative charge

associated with either a reduction of fixed positive oxide charge or an increase in filled acceptor type states situated deep inside the SiC band-gap and/or negative charge build-up related to near-interfacial electron traps [29, 62]. In contrast, NO annealing of dry oxides tends to shift the flat-band voltage towards more negative values and has been attributed to the decrease in trapped negative charge at the interface due to the passivation effects of nitrogen and the net decrease of D_{it} [63]. Over oxidation of an implanted Gaussian N-profile also generates a negative flat-band voltage shift and reduces D_{it} however this effect has been attributed to a large density of fixed positive oxide charges in the oxide and/or near the SiC/SiO2 interface [64]. Positive shifts on the other hand are particularly evident in wet oxidations, apparently as a result from hydrogen related species such as –OH bonds [11, 16, 65, 66]. These shifts have been generally attributed to a larger density of deep acceptor type states. Even after annealing in NO the positive shift has shown to persist however the D_{it} between 0.1 - 0.6 eV from the conduction band has shown significant improvement [33]. Since the low partial pressure oxidation processes occurred in a dry environment the effects of hydrogen can be systematically ruled out.

There seems to be quite some uncertainty in determining the actual cause of the flat-band voltage shift. This highlights the fact that the positive oxide charge and filled deep acceptor states cannot be easily separated due to the overall charge compensation effects that occur. While an overall increase in deep acceptor states cannot be entirely ruled out there seems to be sufficient evidence through the C–V and G–V measurements in Fig. 4.7 to indicate an overall improvement of the SiC–SiO_2 interfacial properties through the reduction of negatively charged acceptor type states associated with the nitridation processes. This is consistent with the improvements reported for NO annealed dry oxides [63]. Therefore the modest positive flat-band voltage shift, as a result of the net increase in negative charge, is

attributed to a reduction in fixed positive oxide charge rather than a larger density of slow, filled acceptor type states.

The exact cause of the positive charge reduction is not exactly clear from the presented results however it can be speculated that this effect is a result of the complex oxidation-nitridation mechanisms at low partial pressures that decouple the growth rate from the influence high temperature resulting in a slow but orderly development of an enhanced SiC–SiO_2 interface.

Gate Oxide Integrity Measurements

Current–voltage measurements were performed under positive gate bias at room temperature in order to compare gate oxide conduction characteristics and access oxide integrity. From the gate area (0.0025cm^2) and the equivalent oxide thickness the current-voltage data was converted into typical semi-logarithmic plots of oxide leakage-current density versus oxide electric field presented in Fig. 4.9 The electric field across the oxide was determined from Eq. (4.2). From the data displayed in Fig.4.9 it can be observed that the turn-over electric field, where the F–N conduction mechanism begins to dominate, is increased for the oxide processes incorporating NO. This implies that a larger range of operational gate voltages can be reliably applied to these gate oxides before degradation of the oxide occurs due to F–N electron injection. To approximate the barrier height between the 4H–SiC/SiO_2 conduction bands, F–N analysis was performed using the high-field regions of I–V plots where F–N tunneling was identified as the dominant conduction mechanism.

At low temperatures, the classical expression for F–N tunneling of electrons from the substrate conduction band through a triangular barrier into the oxide conduction band at room temperature is obtained from the tunneling emission current density in the form [67, 68],

$$J = AE_{ox}{}^{2} \exp(-B/E_{ox}) \tag{4.3}$$

where

$$A = \frac{q^3 m_{SiC}}{(8\pi h m_{ox} \Phi_B)} \tag{4.4}$$

and

$$B = \frac{4(2m_{ox})^{1/2} \Phi_B{}^{3/2}}{(3qh/2\pi)} \tag{4.5}$$

In Eqs. (4.4) and (4.5), m_{SiC} and m_{ox} correspond to the effective electron

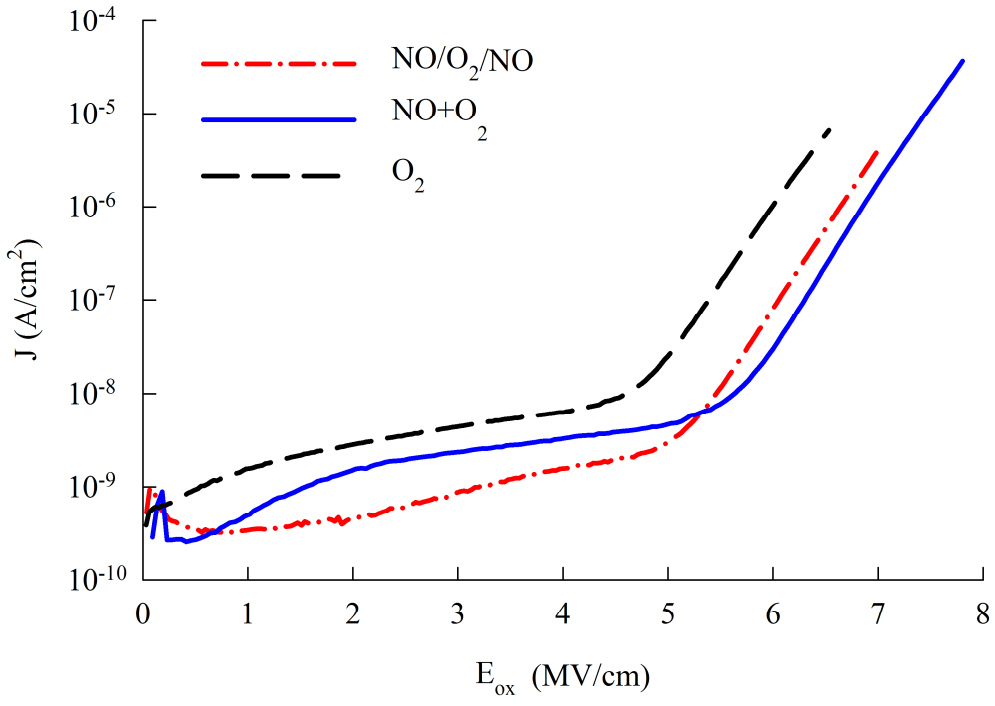

Figure 4.9 Oxide leakage current density as a function of applied electric field at 25°C for N-type 4H–SiC MOS capacitors.

mass in the SiC and SiO_2, respectively, q is the unit electron charge, h is Planck's constant and ϕ_B is the effective barrier height between the conduction bands of the SiC and SiO_2.

The F-N current is strongly dependent on the barrier height which can be determined from the extraction of the so called pre-exponential and exponential coefficients by re-arranging Eq. (4.3) to the following form:

$$\ln\left(J/E_{ox}{}^2\right) = \ln A - B/E_{ox} \qquad (4.6)$$

From Eq. 4.6 the Fowler-Nordheim tunneling current is represented by the linear relationship revealed from a $ln(J/E_{ox}{}^2)$ vs $1/E_{ox}$ plot, whereby the slope is equal to –B.

The Fowler–Nordheim plots corresponding to the reduced I–V data

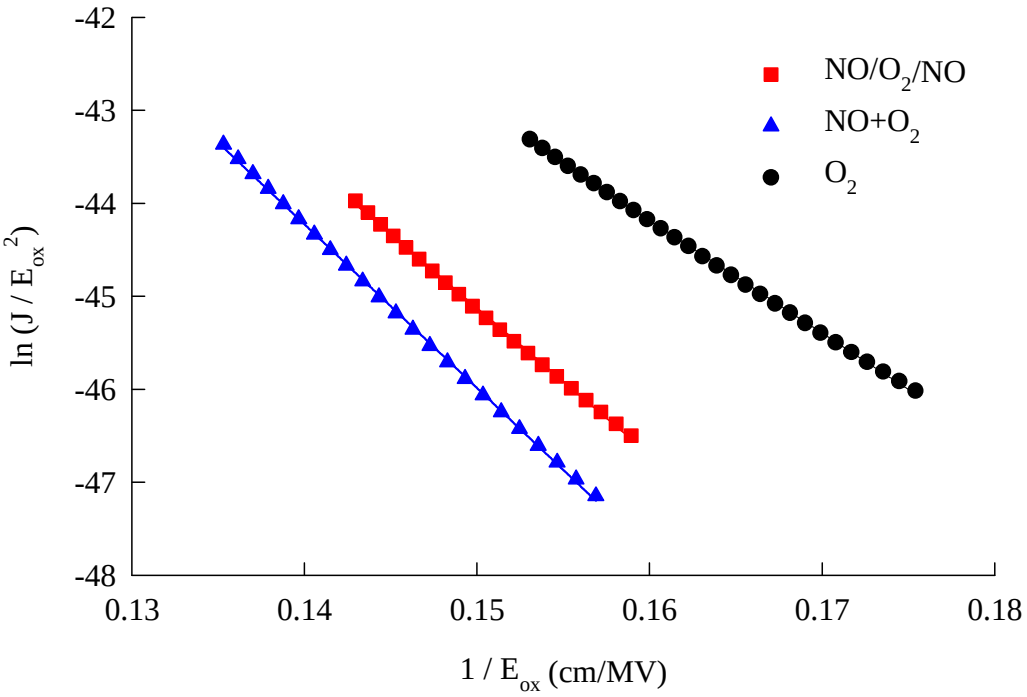

Figure 4.10 Fowler-Nordheim electron injection plots obtained from the J–E_{OX} measurements displayed in Fig. 4.9.

measured at room temperature are illustrated in Fig. 4.10. In all oxides the well-defined linear relationship reveals that the conduction mechanism is dominated by F–N electron injection tunneling mechanism from the SiC

TABLE 4.3. Effective barrier heights for 4H–SiC gate oxides at 25 °C.

	Oxidation Process			
	Theoretical	O_2	$NO/O_2/NO$	$NO+O_2$
ϕ_B (eV) @ 25°C	2.70	1.95	2.33	2.50

substrate into the gate oxide at high electric fields. From the slope of the linear regions, the effective barrier heights were estimated using Eq. (4.6) and summarized in Table 4.2. The value of m_{ox} was approximated as 0.42 m_o [67, 69].

As anticipated from the J–E_{ox} data, both NO-nitrided oxides demonstrate an increase in effective barrier height compared to the dry O_2 reference. The sandwich $NO/O_2/NO$ process yields an accumulative increase of ~ 19 % whereas the combined $NO+O_2$ process yielded a further improvement of ~ 28% with an estimated effective barrier height of 2.50 eV, only ~ 0.2 eV lower than the theoretical ideal value of 2.73 eV [24]. While improvements of oxide electron injection characteristics are synonymous with post oxidation effects of nitridation [69-71], these results also indicate that NO nitridation throughout the oxide growth process at extremely low partial pressure is quite effective in terms of improving the oxide integrity.

The barrier height is fundamentally deduced from the conduction band offset between the SiC substrate and the dielectric. It has been considered that the density and location of interface states in the SiC band-gap can actively influence the F–N tunneling current at the SiC/SiO_2 interface[72]. Internal Photoemission (IPE) spectroscopy studies by

Afanas'ev *et al.* [18] suggests that the presence of carbon cluster like defects (e.g. graphite) whose density is sensitive to processing conditions such as thermal oxidation and ozone cleaning [25] may assist F-N tunneling into the oxide due localised barrier lowering. Therefore the barrier height, rather than being well defined by the difference between the conduction band offsets of the SiC and SiO_2, is essentially reduced due to the density and location of the states aligned to the SiC energy gap and a lower 'effective' barrier height is observed [70]. This hypothesis is warranted through the interfacial characterisation of the previous section where a significant improvement of interfacial properties was observed for those processes treated in NO at low partial pressure through a noticeable reduction of near-interface traps aligned to the conduction band as well as a reduction of states aligned to the SiC energy gap. Combined with the improvements in effective barrier heights, these observations strongly suggest an improved SiC–SiO_2 interfacial region as a result of NO-nitridation.

SUMMARY

Beginning with an overview of SiC oxide growth kinetics and the formation of electrically active defects at the SiC–SiO_2 interface, this chapter focussed on gate oxide nitridation as the most widely accepted method to achieve acceptable SiC–SiO_2 interfacial properties and satisfactory channel-carrier mobilities that has led to the fabrication of commercially viable SiC MOSFETs in recent years. Based on a review of gate oxide nitridation techniques, it was found that oxides directly grown in pure NO exhibit superior SiC–SiO_2 interfacial properties in comparison to post-oxidation annealing of standard thermally-grown oxides in NO, implying that NO-nitridation may be required throughout the SiC oxide growth process to further improve the quality of the SiC–SiO_2 interface. However, the extremely slow growth rate, the toxicity and the amount of NO gas required

particularly in large, production-type oxidation furnaces to fabricate thick gate oxides for SiC power MOSFETs makes the direct growth of gate oxides in pure NO unfeasible. To address these issues, the effects of gate oxide nitridation using a very low partial-pressure of NO via a sequential nitridation/oxidation/nitridation sandwich type process and a novel, combined nitridation/oxidation process were investigated in this chapter.

By employing conventional MOS analysis techniques as well as examining the accumulation conductance-frequency response and F–N analysis of oxide leakage currents it was found that significant improvements of the SiC–SiO_2 interface and oxide integrity were still observed by incorporating gate oxide nitridation in NO at an extremely low partial pressure of 2%. Conventional analysis of C–V curves measured over an array of frequencies revealed that the combined NO+O_2 process exhibited the least frequency dispersion, followed by the NO/O_2/NO *sandwich*-type process. This result was also correlated to the lowest effective interface trapped charge obtained at flat-band and the lowest conductance peaks, all of which indicating a significant reduction in the density of defects energetically located near the 4H–SiC conduction band, within the 4H–SiC bandgap.

Using the novel understanding and detection technique developed in Chapter 3, the NITs aligned to the conduction band between oxide growth processes were also comparatively assessed from a series of accumulation conductance measurements. Both oxides incorporating nitridation demonstrated a considerable reduction in the measured accumulation conductance over the examined measurement frequency range, demonstrating that NO at low partial pressure also effectively reduces the NITs aligned to the conduction band that are particularly detrimental to the channel-carrier mobility in SiC MOSFETs. While both nitrided oxides demonstrated a clear reduction in the NITs aligned to the conduction band,

the combined NO+O_2 process exhibited greatest net improvement. Moreover, these measurements also demonstrate that the accumulation conductance is process dependent, providing experimental evidence that the conductance measured in SiC MOS capacitors biased to accumulation is associated with electrically active defects near the SiC–SiO_2 interface as opposed to the effects of parasitic series resistance.

Besides enhancing the electrical properties of the SiC–SiO_2 interface qualities, NO nitridation at extremely low partial pressure also appears to considerably improve the oxide integrity. Barrier heights extracted from F–N analysis demonstrate that both nitridation processes significantly increase the conduction band offset between the SiC and SiO_2, with the combined NO+O_2 process exhibiting a barrier height of only 0.2eV less than the theoretical value.

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5

CONCLUSIONS AND RECOMMENDATIONS

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5.1 CONCLUSIONS

The research findings presented in this thesis have provided several key contributions towards a better understanding of the SiC–SiO_2 interface in SiC MOS structures. The electrically active defects directly responsible for degrading the channel-carrier mobility in 4H–SiC MOSFETs have been identified and a novel technique to detect these defects in 4H–SiC MOS capacitors has been proposed and experimentally demonstrated. With a better understanding of defects at the SiC–SiO_2 interface two alternative gate oxide growth processes have been proposed to overcome the practical limitations associated with current NO-nitridation techniques in high-volume, production based oxidation furnaces. This work therefore contributes to the wider research effort towards improving the performance

of SiC MOSFETs in several ways. The following paragraphs summarise the key conclusions that have been obtained as a result of this study.

Electrically Active Defects and the Channel-Carrier Mobility (Chapter 3)

A critical review of defects at the SiC–SiO_2 interface exposed a few key discrepancies in both the current understanding of the dominant defects responsible for channel-carrier mobility degradation in 4H–SiC MOSFETs and in the current approach to characterise and evaluate the SiC–SiO_2 interface. Firstly, it was recognised that the Shockley-Read-Hall statistical model, based on thermally activated transport for traps spatially located at the semiconductor-oxide interface, cannot be directly applied to describe the transfer mechanism between free conduction band electrons and the shallow NITs near E_C. This implication tends to suggest that the NITs near E_C in SiC MOS structures cannot be accurately examined using traditional MOS characterisation techniques that are based on this statistical model. Secondly, in accordance with the studies conducted by Saks et. al. [1-3], it was realized that channel-carrier mobility degradation in 4H–SiC MOSFETs is primarily due to the significantly reduced free electron density in the inversion channel. In light of this understanding, the interfacial defects that actively trap channel electrons under *strong inversion* conditions were considered to be dominant in these devices as opposed to the NITs near E_C that are typically examined using conventional MOS characterisation techniques on *N*-type MOS capacitors in *depletion*. To further support this hypothesis, a theoretical analysis of the inversion carrier concentration using the charge sheet model was conducted to demonstrate that the NITs with energy levels corresponding to strong inversion are of key importance to the channel-carrier mobility.

Considering the quantum confinement of carriers in an inversion channel under strong inversion conditions positions the Fermi level well

above E_C, the NITs energetically aligned to the conduction band were identified as the dominant defects that actively degrade the channel-carrier mobility in 4H–SiC MOSFETs. Given their energetic position, quantum mechanical tunneling was proposed as the transfer mechanism between the free channel electrons and these NITs. The wider implication of this hypothesis is that the thermally activated transfer process, frequently presented in the literature, is unrelated to the electrically active NITs aligned to the conduction band.

In view of the observed similarities between the Fermi level of *N*-type MOS capacitors in accumulation and *N*-channel MOSFETs in strong inversion, a novel technique based on the conductance measurements of *N*–type MOS capacitors in accumulation to detect the NITs aligned to the conduction band was proposed and experimentally demonstrated. The accumulation conductance measured in 4H–SiC MOS capacitors was found to be temperature independent, supporting the proposed model in which the transfer mechanism between the channel-carriers and the active NITs is by direct tunneling. In this technique, the measured accumulation conductance is representative of the NITs in partial response to the measurement signal and the measurement signal frequency is representative of the NIT-carrier tunneling time and tunneling distance from the SiC–SiO_2 interface. Therefore this technique provides a simple and direct means of comparatively evaluating the SiC–SiO_2 interface quality and assessing the effectiveness of interface passivation techniques on SiC MOS structures in terms of the electrically active NITs that degrade the channel-carrier mobility in 4H–SiC MOSFETs.

NO-Nitridation at Low Partial-Pressure (Chapter 4)

The effects of NO-nitridation at low partial pressure were investigated to address the practical constraints of NO for the growth of gate oxides in

large production based oxidation furnaces. A series of 4H–SiC gate oxides were grown using a novel, combined $NO+O_2$ process and a sequential $NO/O_2/NO$ *sandwich* type process in an 8" production based atmospheric oxidation furnace, employing NO at an extremely low partial pressure of 2%.

The novel understanding of the defects that actively degrade the channel carrier mobility in SiC MOSFETs proposed in the previous chapter was successfully applied to comparatively evaluate the effectiveness of NO-nitridation at low partial pressure in the passivation/removal of the NITs aligned to the conduction band in these oxides. By comparing the measured accumulation conductance at a nominal oxide field of 1.5 MV/cm, to avoid oxide thickness discrepancies, it was clearly observed that NO-nitridation at low partial pressure was effective in reducing the measured conductance over the examined measurement frequency range in both nitrided gate oxides, implying a reduction in the near-interfacial defects that are particularly detrimental to the channel-carrier mobility. Using this technique it was found that the oxide grown in a combination $NO+O_2$ process exhibited the best interfacial properties. This finding was further supported through the conventional analysis of *C–V* and *G–V* curves which indicated that the $NO+O_2$ grown oxide exhibited the least frequency dispersion, the lowest effective interface trapped charge obtained at flat-band and the lowest conductance peaks, in comparison to the oxide grown by the sandwich process. The enhanced quality of the $SiC–SiO_2$ interface was related to the various mechanisms surrounding nitrogen incorporation at the interface which retard the oxide growth rate as clearly observed.

In addition to improving the $SiC–SiO_2$ interface it was also shown that NO-nitridation at low partial pressure enhances the oxide integrity by providing greater immunity to electron injection mechanisms. Employing Fowler-Nordheim analysis, the conduction band offset between the SiC and

SiO_2 was estimated at 2.33 eV and 2.50 eV for the $NO/O_2/NO$ and $NO+O_2$ grown oxides respectively, representing an enhancement of ~19 % and ~28 % over non-nitrided gate oxides grown under similar conditions.

These promising results highlight the beneficial effects of NO-nitridation even at extremely low partial-pressure and in the presence of O_2, throughout the gate oxide growth process. The low partial-pressure NO-nitridation processes investigated in this study substantially reduces the amount of NO required, which is a favourable consideration for the growth of gate oxides in large production based furnaces, while improving the electrical quality of the $SiC–SiO_2$ interface and overall integrity of the thermally grown oxide layer.

5.2 SUGGESTIONS FOR FUTURE RESEARCH

In this thesis, a technique to detect the electrically active defects in SiC MOS structures that are directly responsible channel-carrier mobility degradation in 4H–SiC MOSFETs has been established and was successfully applied to demonstrate the effectiveness of NO-nitridation at low partial pressure on enhancing the quality of the $SiC–SiO_2$ interface. These outcomes are of practical significance toward a better understanding the $SiC–SiO_2$ interface and the realization of power MOSFETs that can fully exploit the material advantages of SiC. In order to make further progress toward this wider research effort, several implications and aspects of the work presented in this thesis that warrant further investigation have been identified and summarized in the following paragraphs.

- *The influence of the NIT spatial location on the channel-carrier mobility requires assessment:*

  As observed in Chapter 4, the measured accumulation conductance-frequency profiles were dependant on the gate oxide growth process.

The superior process was determined from the greatest net reduction in the accumulation conductance over the examined measurement frequencies and further supported by conventional MOS characterisation techniques. However it is yet unknown how the spatial distribution of the NITs aligned to the conduction band (corresponding to the measurement frequency) affects the channel-carrier mobility in SiC MOS devices. Given the significant differences observed in the accumulation conductance–frequency profiles of these oxides, this aspect requires further analysis and investigation to determine any dominance relating to the physical location of the electrically active defects.

- *Determining the NIT density and spatial location:*

  In its current form, the proposed technique provides both an indication of the density and spatial distribution of the NITs aligned to the conduction band from the measured accumulation conductance–frequency profiles of *N*–type MOS capacitors. This technique was successfully applied in Chapter 4 to comparatively evaluate the effectiveness of gate oxide growth processes on improving the quality of the SiC–SiO_2 interface. With further work, the density of NITs could be determined from the accumulation conductance and the NIT–carrier tunneling distance calculated from the measurement frequency to qualitatively analyse the SiC–SiO_2 as a stand-alone characterisation method that could be widely adopted in the SiC community. Obtaining a direct correlation between the NIT density and the channel-carrier mobility in SiC MOSFETs would further strengthen this method.

- *Gate oxide growth process optimization:*

  It has been demonstrated that gate oxide growth in a combination of 2 % NO and 5% O_2 significantly improves the quality of the SiC–SiO_2 interface and the integrity of the oxide layer. Given the extremely low partial pressure and thus relatively small amount of NO required throughout this process, it provides a practical avenue for further investigation and development of gate oxidation processes, such as the study of different NO/O_2 ratios in order to optimize this process. This could be combined with physical analysis techniques like SIMS and XPS to determine the amount of nitrogen incorporated at the SiC–SiO_2 interface and the bonding arrangements as a result of gate oxide nitridation in the presence of oxygen.

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