Fast EMC Modelling and Optimization for Reducing Capacitances of Interconnections with Arbitrary Shape in Multilayer VLSI Circuits

Boyuan Zhu[1], *Student Member*, *IEEE*, Junwei Lu[1], *Senior Member*, *IEEE*, and Mingcheng Zhu[2], *Fellow*, *IEEE*

[1]School of Engineering, Griffith University, Brisbane, QLD 4111, Australia
[2]College of Information Engineering, Shenzhen University, Shenzhen, 518060, P.R.China

This paper presents an EMC modelling method for the purpose of calculating the interconnect capacitance between VLSI interconnects based on the finite element method (FEM). Two- and three-dimensional interconnect modelsare simulated and the results of capacitance extraction are compared with experimental measurements, which proved the consistency and accuracy of FEM. Furthermore, optimizations of coupling capacitance are applied on two- and three-dimensional multilayer interconnection structures by the non-dominated sorting genetic algorithm II (NSGA-II), whichshows a capacity foroptimization. They are applicable to arbitrary structures in very-large-scale-integration (VLSI).

Index Terms—Coupling Capacitances, EMC Modelling, Integrated Circuit Interconnections, Structure Optimization

I. INTRODUCTION

Due to the exponential increases in transistors within VLSI circuits, the interconnect power dissipation turns out dynamically in total percentage of power consumption[1]. It is the faster switching activities of interconnect capacitances, with larger numbers of interconnects, which increase power consumption. In this case, the prediction of interconnect capacitances in the layout design phase will lead to a time and cost saving during the entire VLSI circuit production period. However, to date, capacitance calculation of interconnection is inefficient because of its smaller size, multiple metallization layers, reduced routing distance, complex materials and increased working frequencies [2]. Conventional extraction of interconnect capacitance of VLSI is at circuit level or empirical based equations [3].They are not sufficient for complicated structures. Therefore, a fast and accurate modelling approach of interconnects for VLSI is becoming more significant for calculating interconnect capacitance.

Fig.1 provides a general example of capacitance components for parallel and crossover interconnects inside VLSI. Coupling capacitance is one of the major parameters relating to crosstalk noise that consumespower and affectsdelay and signal integrity. It virtually exists only between adjacent interconnects or crossing interconnects. In this paper, a numerical method is applied to obtainan accurate solution of capacitance computation forelementary structures for VLSI. Optimizations of two- and three-dimension multilayer interconnect structures are processed by a fast multi-objective evolutionary algorithm (MOEA), NSGA-II.

II. THEORETICAL BACKGROUND

A. Capacitance Calculation Methodology

An accurate and fast method of calculation is to apply the principle of energy conservation using electrical field energy stored in the volume V. The electrostatic energy of a linear N electrode (the Nth is ground) system is:

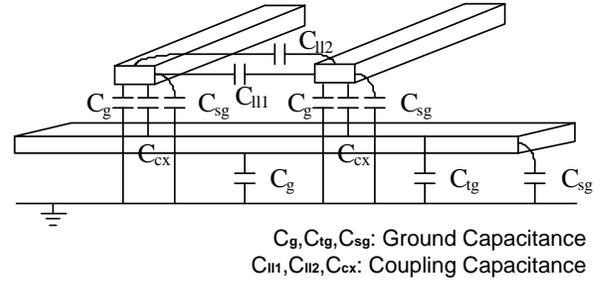$$W = \frac{1}{2}\sum_{i=1}^{N}C_{ii}^{g}V_i^2 + \frac{1}{2}\sum_{i=1,j=1,i\neq j}^{N}C_{ij}^{g}V_iV_j \qquad (1)$$

Fig.1 Example of an interconnect capacitance.

where, W is electrostatic energy; V_i or V_j is the potential of the ith electrode with respect to the ground; C_{ii}^{g} is the self ground capacitance of the ith electrode and C_{ij}^{g} (i $\neq$ j) is the mutual ground capacitance between electrodes. By applying appropriate voltages on electrodes, the coefficients of the ground capacitance can be calculated from the stored static energy.

B. Multi-objective Optimization Algorithm - NSGA-II

As an improved version of a non-dominated sorting genetic algorithm (NSGA), NSGA-II performs a fast multi-objective evolution in terms of finding a diverse set of solutions and in converging near the true Pareto-optimal set [4]. There are several concepts that need explaining.

Non-dominated dominance and non-dominated set: When neither vector is better than the other in every dimension, they are non-dominated with each other. A non-dominated set refers to any two vectors that are non-dominated with each other in a group of vectors.

Pareto front: In the objective space, the global non-dominated point set is called the Pareto front. Without further information, multi-objective optimization algorithms try to obtain a uniform sampling over the Pareto front.

Non-dominated ranking: When dividing a group of vectors into different layers (in terms of non-dominated dominance), any one individual in the sub-group withthe higher rank will dominate every vector in the sub-group with the lower rank, while the individuals in each sub-group are non-dominated with each other.
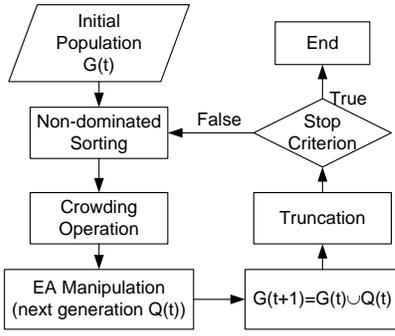
Fig.2 A flow chart of the NSGA-II process.

Crowding distance: This is a new parameter, which is calculated for each individual in order to measure its distance from its neighbours. The larger average crowded distance results to better diversity of population.

The main optimization procedure of NSGA-II is described in a flow chart shown in Fig.2. The first step initializes the population (size N) based on the defined problem range and constraints. Non-dominated sorting is then applied to the initialized population, which is sorted based on non-domination into each front. The first front is a completely non-dominant set in the current population while the second front is dominated by the individuals in the first front only, and so on. When non-dominated sorting is complete, the crowding distance is calculated and assigned for all individuals in the population. Based on the rank and crowding distance, parents are selected for evaluation manipulation, which generates the offspring population. The current population and generated offspring will be combined again based on the non-domination. Only the best N individuals are selected for the new population and others are truncated. Thus, iterations continue until the stop criterion is achieved.

III. NUMERICAL SIMULATION AND STRUCTURE OPTIMIZATION

The following simulation and optimization are performed with Intel® Core ™ Duo CPU E8400 @ 3.00 GHz and 4.00 GB Memory.

A. Model Simulation and Verification

Fig.3 presents some typical models of interconnect structures. These include different interconnects wiring in two-dimensional parallel and overlapping structures, and three-dimensional crossover structures.

As listed in TABLE I, the capacitance of the interconnect is calculated and compared with the semi-empirical model and measurement results from Wong et al. **Error! Reference source not found.**. The measurement data us collected by HP4284. In TABLE II, the corresponding CPU runtime with element number and type are presented. For the parallel structure in Fig.3 (a), the self-capacitance of conductor 2 is used for comparison. For the overlapping structure in Fig.3 (b), when distance 0>d>-1.8, the two interconnects overlap. In addition, the self-capacitance of conductor 1 in Fig.3 (c) is used for comparison. As the overlapping area deceased, self-capacitance is consequently decreasing. FEM is proved correct and leads to a more
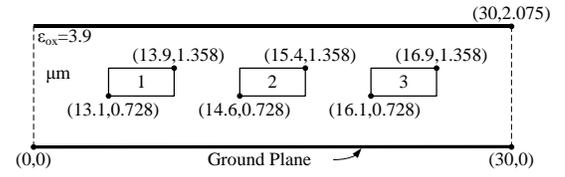
(a) 2D structure of three parallel interconnects between two ground planes.
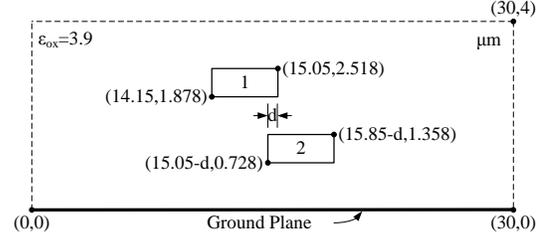
(b) 2D structure of two overlapping interconnects on different layers.
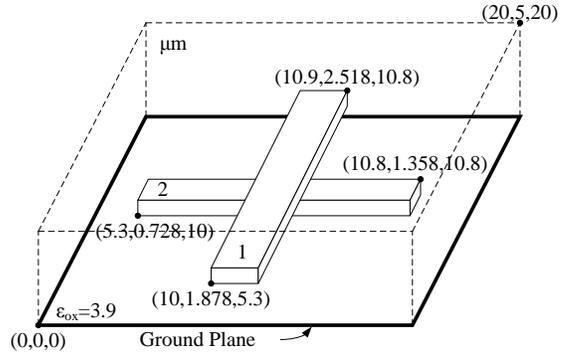
(c) 3D structure of crossover interconnects in one dielectric.

Fig.3　Structure of different interconnects wiring.

TABLE I
EXPERIMENTAL RESULTS OF DIFFERENT INTERCONNECTS WIRING(FF/μM)

Structure	Semi-empirical Model Error! Reference source not found. and Accuracy v.s. Measurement	FEM and Accuracy v.s. Measurement (This paper)	Measurement Error! Reference source not found.
(a)	0.216 (-7.9%)	0.214 (-8.9%)	0.233
(b) d=0	0.121 (+15.2%)	0.119 (+11.8%)	0.105
(b) d=0.4	0.136 (+11.8%)	0.132 (+10.0%)	0.120
(b) d=0.8	0.146 (+14.1%)	0.139 (+8.5%)	0.128
(b) d=-0.4	0.116 (+25.9%)	0.107 (+19.6%)	0.086
(c)	0.736 (-11.1%)	0.8044 (-1.7%)	0.818

TABLE II
SIMULATION ELEMENT AND CPU RUNTIME

Structure	Element Number	Element Type	CPU Runtime
(a)	5296	2D Triangle	7.776
(b) d=0	5056	2D Triangle	5.062
(b) d=0.4	5048	2D Triangle	5.000
(b) d=0.8	5072	2D Triangle	5.062

accurate result. This shows that FEM provides a result that is 10% closer to the measurement compared to the semi-empirical model.

B. Optimization

With the help of commercial software, such as Matlab and FEM solver, the objective of this research is to reduce parasitic capacitances of interconnects by optimizing the
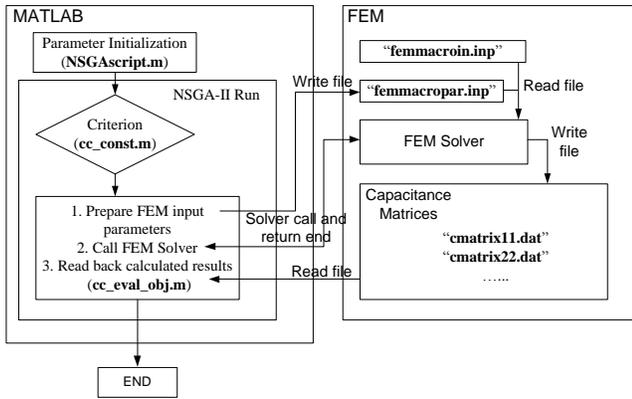
Fig.4 Optimization program interaction between Matlab and the FEM.

structure of the multi-conductor. A specialized multi-objective program is used for the purpose of optimization in different interconnects. presents an operational diagram demonstrating the interaction between Matlab and FEM during the optimization procedure. Matlab is the main body of the optimization program (NSGA-II) and FEM is in charge of calculating the interconnect capacitances. In this part, optimization in 2D is given. NSGAscript_2D.m defines all input ranges used in optimization and then usesthe main body of the NSGA-II program. To select the valid structuralparameters, criterion (cc_const_2D.m) is defined by user and processed before calculation. In the process of optimization, cc_eval_obj_2D.m prepares input structural parameters for FEM and writes them into femmacropar.inp. When FEM is called in batch mode, it runs amacro called femmacroin_2D.inp,which automatically reads the defined parameter. After the calculation is done, it writes the obtained capacitance matrices into different groups of files. When Matlab detects the completion of FEM, it reads back the matrices and proceeds to the next step of EA manipulation.

With different conductor positions, the total ground capacitance and the total coupling capacitance for interconnects are varied. The aim of this optimization is to find the best allocation of conductors, which contributes to the lowest value for the trade-off between total ground capacitance and total coupling capacitance of interconnects. The initial value of the population is randomly assigned by the optimization program. Sufficient generations are iterated to ensure the optimization result is converged. Only the most satisfactory result from a group of multi-objective results is selected and shown in the following section below.

1) 2D Multi-layer interconnects of VLSI

With the NSGA-II algorithm, an optimized capacitance result of interconnects can be obtained. For example, in the overlapping structure in Fig.3 (b), optimization is needed on the coupling capacitance between conductors 1 and 2, which are constrained within Layer1 and Layer2, as shown in Fig.5. It is found that coupling capacitance C12 or C21 reduced from 0.93111E-4 pF to 0.19336E-7 pF per unit length (in μm). It proves that the optimization program is working effectively.

Fig. 6 shows an advanced 2D multi-layer structure for interconnects of VLSI. There are five levels of conductors inside two isolated layers upon a silicon substrate. Each layer
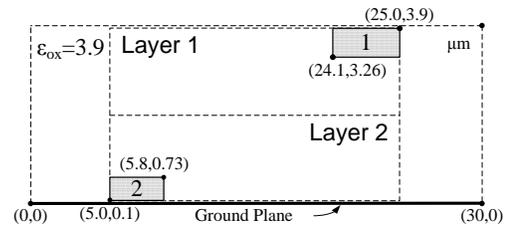

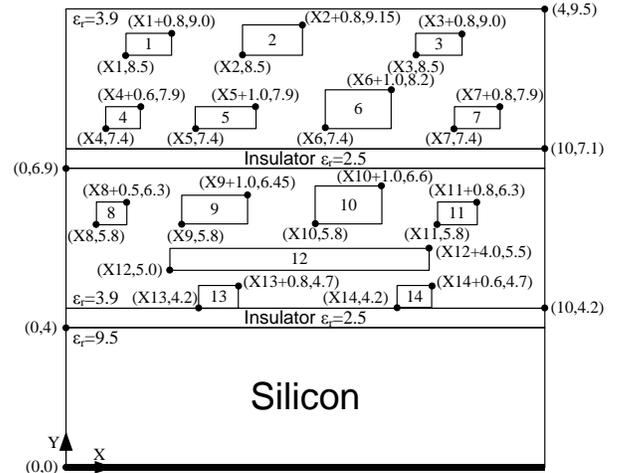Fig.5 Capacitance optimization of overlapping interconnects.

Fig.6 2D multi-layer interconnects for optimization.

TABLE III
OPTIMIZED RESULT OF TARGET MATRIX (μM)

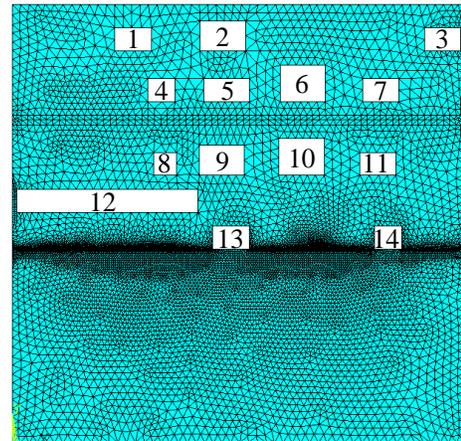| X1	X2	X3	X4	X5	X6	X7
2.27	4.15	9.1	3	4.23	5.91	7.73
X8	X9	X10	X11	X12	X13	X14
3.13	4.13	5.89	7.67	0.1	4.43	8

Fig.7 Optimization results of 2D multi-layer interconnects.

is isolated by a low permittivity material. The population G(t) for optimization is the matrix of [X1,X2,…,X14], as shown in the layout figure. Each individual simulation takes 261.922 CPU runtime with 19736 triangle elements.

The total ground capacitance obtained is 2.29E-03 pF/μm and total coupling capacitance is 2.21E-03 pF/μm. An optimized matrix is obtained and presented in TABLE III. It contributes to the optimized structure as shown in Fig.7. As illustrated, conductor 12 is shifted to the boundary side in
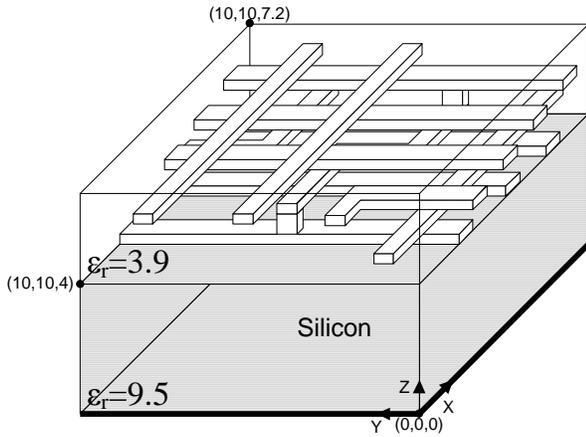
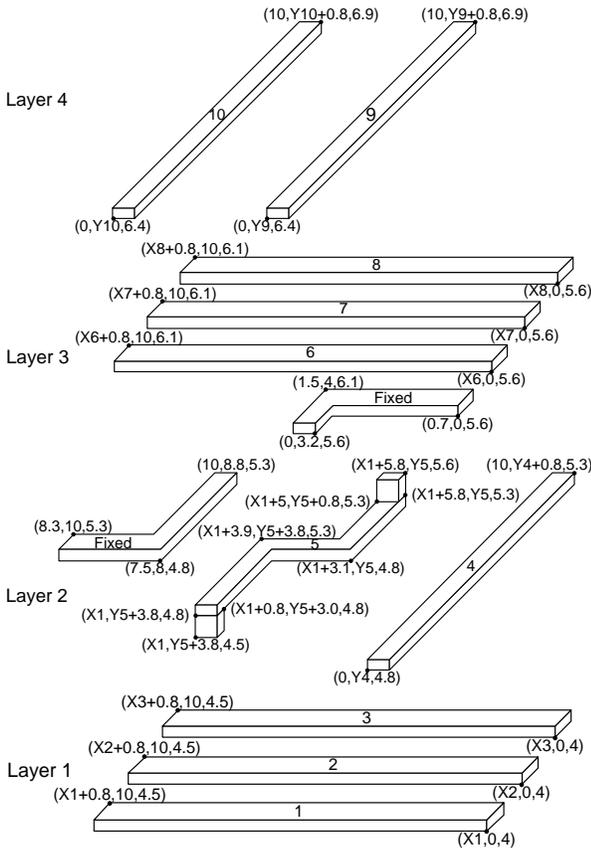Fig.8 3D multi-layer interconnects for optimization.

Fig.9 Dimension details of 3D multi-layer interconnects.

order to avoid overlap with other conductors. The overlapping area of conductor 12 contributes to a large percentage of total coupling capacitance.

2) 3D Multi-layer interconnects of VLSI

There is a 3D multi-layer interconnect structure for VLSI, as shown in Fig.8. Twelve interconnects are routed within four different layers. The layout details for each layer are described in Fig.9. The optimization population in this case is the matrix of [X1,X2,X3,Y4,Y5,X6,X7,X8,Y9,Y10]. Each individual simulation costs 153.234 CPU runtime with 21199 triangle elements.

According to the optimized result, the total ground

TABLE IV
OPTIMIZED RESULT OF AXES MATRIX (μM)

X1	X2	X3	Y4	Y5
1.53	6.52	9.1	0.1	3.52
X6	X7	X8	Y9	Y10
1.99	3.51	6.53	0.1	9.1

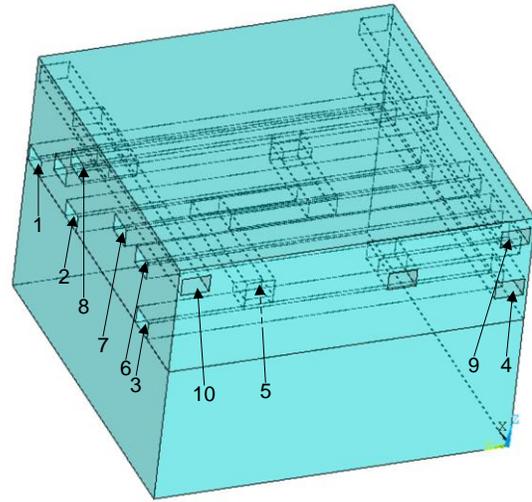
Fig.10 3D multi-layer interconnects for optimization.

capacitance obtained is 1.64E-02 pF/μm and total coupling capacitance is 1.48E-02 pF/μm. The corresponding structural parameter is listed by the matrix in Table IV. The final optimized 3D structure is consequently plotted, as shown in Fig.10. According to the figure, all parallel interconnects are separated widely to avoid coupling capacitance between each other. In addition, the structural width of interconnects 9 and 10 minimized overlapping coupling capacitance compared with interconnect 5 and two other fixed "L" shape interconnects.

IV. CONCLUSION

In this paper, a fast EMC modelling approach is proposed to calculate the capacitance of interconnects for VLSI circuits and a novel genetic evolutionary algorithm optimization is undertaken which aims at optimizing the arbitrary structure of VLSI interconnects within 2D and 3D to minimize capacitive coupling effects among interconnects.

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