Extraction of MOSFET threshold voltage, series resistance, effective channel length, and inversion layer mobility from small-signal channel conductance measurement

Author
Kong, Frederick Chung Jeng, Yeow, Y. T., Yao, Z. Q.

Published
2001

Journal Title
IEEE TRANSACTIONS ON ELECTRON DEVICES

DOI
https://doi.org/10.1109/16.974720

Copyright Statement
Copyright 2001 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

Downloaded from
http://hdl.handle.net/10072/55879
Extraction of MOSFET Threshold Voltage, Series Resistance, Effective Channel Length, and Inversion Layer Mobility From Small-Signal Channel Conductance Measurement

F. C. J. Kong, Y. T. Yeow, Senior Member, IEEE, and Z. Q. Yao, Member, IEEE

Abstract—This paper proposes and demonstrates the extraction of MOSFET threshold voltage, source-drain resistance, gate field mobility reduction factor, and transistor gain factor from the measurement of the small-signal source-drain conductance of a transistor as a function of dc gate bias with zero dc drain bias. The theory is based on the analytical model that includes the effects of source-drain resistance and gate-induced mobility reduction. It is shown that, by measuring devices of different drawn gate lengths, effective channel lengths and actual mobility can also be extracted. The results obtained are compared with those obtained by other measurement methods.

Index Terms—MOSFET threshold voltage, parameter extraction, source/drain resistance.

I. INTRODUCTION

THRESHOLD voltage, inversion layer carrier mobility, source and drain series resistance, together with device dimensions, form the major parameters of the SPICE-based submicrometer MOSFET circuit model used in the circuit simulation of MOS integrated circuits. The MOSFET circuit model itself is developed from the analytical model for the drain current (as a function of gate and drain bias) based on the well-known gradual channel analysis of the inversion layer conduction [1]. These SPICE parameters are extracted from different measurements based on the circuit model. The most common measured quantity used for parameter extraction is the dc drain current [2]; more recently, small-signal interelectrode capacitance measurements are also used [3], [4]. Each measurement technique has its advantages and limitations; some are aimed at determination of a single parameter, while others yield a number of parameters simultaneously. Simplicity of measurement and parameter extraction, adaptability to changes in technology, and applicability of the extracted parameters (in terms of variation in device dimensions and bias voltage range) are factors affecting the choice of measurement techniques in practice.

In this paper, we describe a novel and simple method for accurate extraction of threshold voltage \( V_T \), gain factor \( \beta \), gate bias mobility lowering factor \( \theta \), and source/drain series resistance \( R_T \) of a MOSFET from a single measurement of the small-signal ac drain-source conductance \( g_{ds} \), as a function of dc gate bias. As with other SPICE parameter extraction measurements, it is derived from the standard gradual channel theory analysis for \( I_d \) (\( V_{ds} \), \( V_{gs} \)) used in SPICE. The measurement uses only a small (\( \sim 10 \) mV rms) ac signal applied to the drain. With zero dc drain bias, effects such as channel length modulation, drain-induced barrier lowering (DIBL), and carrier velocity saturation on the above four parameters are eliminated.

By carrying out the same measurement for devices with different drawn gate lengths, the method also allows the extraction of the effective channel lengths of the devices and the effective inversion layer mobility.

II. THEORY OF PROPOSED PARAMETER EXTRACTION

The intrinsic small-signal conductance between source and drain of a MOSFET can be derived directly from the dc drain current equation based on gradual channel approximation

\[
g_{ds} = \left[ \frac{dI_{ds}}{dV_{ds}} \right]_{\text{const} V_{gs}} = \left[ \frac{d}{dV_{ds}} \left( \frac{\mu_{\text{eff}} C_{ox} W_{\text{eff}}}{L_{\text{eff}}} \times \left( V_{gs} - V_T - \frac{V_{ds}}{2} \right) V_{ds} \right) \right]_{\text{const} V_{gs}} \tag{1}
\]

where

- \( C_{ox} \), gate oxide capacitance per unit area;
- \( \mu_{\text{eff}} \), low field effective inversion layer mobility;
- \( W_{\text{eff}} \), effective channel width;
- \( L_{\text{eff}} \), effective channel length.

In the measurement described below, zero drain bias is used, i.e., \( V_{ds} = 0 \). This gives the intrinsic \( g_{ds} \) as

\[
g_{ds} = \frac{\mu_{\text{eff}} C_{ox} W_{\text{eff}}}{L_{\text{eff}}} (V_{gs} - V_T) = \beta (V_{gs} - V_T) \tag{2}
\]

where

\[
\beta = \frac{\mu_{\text{eff}} C_{ox} W_{\text{eff}}}{L_{\text{eff}}}. \tag{3}
\]
In actual measurement, the source-drain resistance \( R_T \), being in series with the channel resistance, is included in the small-
signal conductance measured between source and drain. Hence, the
measured small-signal conductance \( g_{\text{dsn}} \) is
\[
 g_{\text{dsn}} = \frac{1}{R_T + \frac{1}{\beta_0 (V_{gs} - V_T)}}. \tag{3}
\]

In SPICE-based modeling, low field inversion mobility is most commonly modeled as being dependent on \( V_{gs} \) according
the functional form \[5\]
\[
 \mu_{\text{eff}} = \frac{\mu_0}{1 + \theta (V_{gs} - V_T)} \tag{4}
\]
where \( \mu_0 \) is the zero gate field mobility and \( \theta \) is the gate-field
mobility reduction factor. When the gate-field dependent expression
for \( \mu_{\text{eff}} \) is introduced into the small-signal conductance
equation, we get
\[
 g_{\text{dsn}} = \frac{\beta_0 (V_{gs} - V_T)}{1 + (\theta + \beta_0 R_T) (V_{gs} - V_T)} \tag{5}
\]
where
\[
 \beta_0 = \frac{\mu_0 C_{\text{ox}} W_{\text{eff}}}{L_{\text{eff}}}.
\]

When \( g_{\text{dsn}} \) is measured as function of \( V_{gs} \), the results
can theoretically be used as the target function to extract the
values of the parameters \( V_T \), \( R_T \), \( \beta_0 \), and \( \theta \) simultaneously
by parameter optimization to fit (5) to the experimental data.
Rather than doing this, we make use of the fact that the function
\[
 \frac{g_{\text{dsn}}}{\sqrt{\frac{dg_{\text{dsn}}}{dV_{gs}}}} \text{ is a linear function in } V_{gs} \text{ in which the}
\]
two parameters \( R_T \) and \( \theta \) are eliminated
\[
 \frac{g_{\text{dsn}}}{\sqrt{\frac{dg_{\text{dsn}}}{dV_{gs}}}} = \sqrt{\beta_0} (V_{gs} - V_T). \tag{6}
\]

This allows for the use of simple straight-line fit to the nu-
merically derived experimental quantity \( g_{\text{dsn}}/\sqrt{\frac{dg_{\text{dsn}}}{dV_{gs}}} \) to extract \( V_T \) and \( \beta_0 \) for a given device. The proposed procedure
for the extraction of \( V_T \) from experimental data is simpler than
other existing methods such as those in \[2\] and \[6\], essentially
due to the avoidance of the use, and hence also the influence of,
dc drain bias. After having determined \( V_T \) and \( \beta_0 \), the two
remaining parameters \( R_T \) and \( \theta \) are extracted by optimization to
fit (5) to the measured data \( g_{\text{dsn}} \).

By carrying out the above measurement and extraction pro-
cedure for devices with different drawn gate lengths \( L_{\text{drawn}} \),
fabricated by the same technology, we obtain the experimental
data \( \beta_0 \) as a function of \( L_{\text{drawn}} \). Adopting the standard relation-
ship between drawn length and effective length of \( L_{\text{eff}} = (L_{\text{drawn}} - \Delta L) \tag{7} \), where \( \Delta L \) taken as a constant, we get
\[
 \beta_0 = \frac{\mu_0 C_{\text{ox}} W_{\text{eff}}}{L_{\text{drawn}} - \Delta L}. \tag{7}
\]

The preceeding equation is the basis of the \( 1/\beta \) method \[8\]:
\( 1/\beta_0 \) is plotted against \( L_{\text{drawn}} \) for the determination of \( \Delta L \) and

- **Fig. 1.** (a) Schematic diagram for the measurement of \( g_{\text{dsn}} \) and (b) small-signal equivalent circuit of transistor with zero drain bias.

\( \mu_0 \) (using known values for \( W_{\text{eff}} \) and \( C_{\text{ox}} \)) from the x-axis intercept and slope, respectively, of the best-fit straight line for the experimental data.

### III. Measurement

Small-signal conductance \( g_{\text{dsn}} \) can be measured directly
using an LCR meter. Fig. 1(a) shows the schematic diagram of the measurement circuit. The HP4284 A LCR meter applies a
test signal of 10 mV rms at 1 MHz at the drain and the signal
current is sensed at the grounded source. Voltage sources of a
HP 4145A parameter analyzer are used to provide the necessary
gate and substrate bias. Fig. 1(b) shows the small-signal equiv-
alent circuit of the measurement. With dc bias \( V_{gs} \) set at zero,
there is no drain current and hence no dc voltage drop across
the source and drain resistances \( r_s \) and \( r_d \) \( (r_s = r_d = R_T/2) \).
Devices under test are LDD n-channel MOSFETs with drawn
length ranging from 0.4 to 20 \( \mu \)m, oxide thickness of 10 nm,
and \( W_{\text{eff}} \) of 20 \( \mu \)m. The experimental \( g_{\text{dsn}} \) is used to extract
parameters according to the theory described above.

Chern’s method \[7\] for the extraction of \( R_T \) and \( \Delta L \) requires
the measurement of the resistance between source and drain
\( R_M \) as a function of \( V_{gs} \) for a number of devices with different
drawn lengths. Other than the fact that \( R_M \) is typically derived
from dc measurement, it is the reciprocal of the small-signal
quantity \( g_{\text{dsn}} \) we measured. Thus, the same set of data can be
processed by Chern’s method to extract \( L_{\text{eff}} \) and \( R_T \) for com-
parison with the values extracted by the proposed method. The
only difference is that in Chern’s method, a single \( R_T \) is ex-
tracted from a set of measured drain-source resistances for de-
vices with different drawn gate lengths, whereas in the proposed
method, one value of \( R_T \) is extracted for each device measured.
The \( V_T \) extracted by the proposed method for each device is
used in Chern’s method. For comparison purposes, \( V_T \)s are also
extracted from dc \( I_d - V_{GS} \) measurement by the linear extrapolation method [2].

### IV. RESULTS AND DISCUSSION

Fig. 2 shows the experimental \( g_{ds,m} \) as a function of \( V_{GS} \) for \( L_{\text{drawn}} = 0.4 \) to 20 \( \mu \text{m} \). Fig. 3 shows \( g_{ds,m}/\sqrt{dg_{ds,m}/dV_{GS}} \) versus \( V_{GS} \) derived from Fig. 2 with \( dg_{ds,m}/dV_{GS} \) calculated using central finite difference. According to (6), the \( x \)-axis intercept and slope of the best straight line fit of the data for each device in Fig. 3 yield the \( V_T \) and \( \sqrt{\beta_0} \) respectively, for that device. The extracted \( V_T \)s as a function of \( L_{\text{drawn}} \) is shown in Fig. 4. The 95%-confidence intervals of \( V_T \) obtained by standard linear regression analysis are shown as error bars in the figure. For all drawn lengths the spread is within 3% of the extracted value. In the same figure, we also show \( V_T \) extracted from \( I_d - V_{GS} \) measurement by the linear extrapolation method [2]. The difference is less than 50 mV.

Next, we proceeded to extract the values of \( R_T \) and \( \theta \) for each device by fitting (5) into the corresponding data in Fig. 2. The extracted values of \( V_T, \beta_0, R_T, \) and \( \theta \) for each device are tabulated in Table I (values in parentheses are results obtained by other methods). Theoretically, \( R_T \) and \( \theta \) are independent of gate length. This is seen to be the case for results obtained by independent parameter optimization on data measured on devices with different \( L_{\text{drawn}} \).

As indicated in the Section II, \( 1/\beta_0 \) is next plotted against \( L_{\text{drawn}} \) to extract \( \mu_0 \) and \( \Delta L \) and hence also \( L_{\text{eff}} \). This is shown in Fig. 5, giving \( \Delta L = 0.00 \mu \text{m} \) and \( \mu_0 = 465 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \).
using the values of $W_{	ext{eff}} = 20 \, \mu\text{m}$ and $t_{	ext{ox}} = 10 \, \text{nm}$ and $L_{	ext{eff}}$s are included in Table I. For comparison, Chern’s method mentioned is carried out using $R_M(=1/g_{\text{km}})$. Results are shown in Fig. 6 for $(V_{\text{gs}} - V_T) = 1, 1.5, 2$ V. The plot yields $R_T = 68 \, \Omega$ and $\Delta L = 0.085 \, \mu\text{m}$. These results are shown in parentheses in the corresponding columns in Table I. It is seen that both parameters are in good agreement with the corresponding values determined by the present method.

Inversion layer mobility for MOSFET as a function of gate bias $\mu_{\text{eff}}(V_{\text{gs}})$ is usually extracted directly from the intrinsic channel conductance $g_{\text{ks}}$ [2]. The inset in Fig. 7 shows the $g_{\text{ks}}$ for the 0.8-µm device obtained from $g_{\text{km}}$ data by the equation: $g_{\text{ks}} = 1/(1/g_{\text{km}} - R_T)$. Using extracted $g_{\text{ks}}, L_{\text{eff}}, V_T$, and the assumed values for $C_{\text{ox}}$ and $W_{\text{eff}}$, we obtained $\mu_{\text{eff}}(V_{\text{gs}})$ from (2). This is shown as points in Fig. 7. It shows the typical dropping off of $\mu_{\text{eff}}$ with reducing $V_{\text{gs}}$ just above threshold observed in measurement using (2). This is attributed to the failure near $V_T$ of the assumption that inversion layer charge $= C_{\text{ox}}(V_{\text{gs}} - V_T)$ [2]. The extracted $\mu_0$ and $\theta$ should also yield mobility through (4). The full line in Fig. 7 shows the calculated $\mu_{\text{eff}}(V_{\text{gs}})$ obtained for the range of $V_{\text{gs}}$ where the experimental $g_{\text{km}}$s are used in our extraction process. Since the difference between the two sets of $\mu_{\text{eff}}(V_{\text{gs}})$ is within 2% for this range of $V_{\text{gs}}$, the dotted line which is the extrapolation (4) should be a good prediction of the actual mobility down to $V_{\text{gs}} = V_T$.

Extraction methods based on dc $I_d$ measurement requires the application a small dc drain bias $V_{\text{ds}}$, typically 50 mV–100 mV. This bias leads to nonuniformity of the inversion layer along the channel as well as other longitudinal field-induced effects such as mobility reduction, channel length modulation and DIBL. By measuring small-signal $g_{\text{ds}}$ with dc drain offset we can monitor these effects in devices with different channel lengths. We extracted the intrinsic $g_{\text{ks}}$ as a function of $V_{\text{ds}}$ offset between 0 and 200 mV for $L_{\text{drawn}} = 0.4$ and 2 µm when the devices are in the linear region of operation. Due to the presence of dc drain current, the effective or the intrinsic dc $g_{\text{dm}}$ and $V_T$ are less than the applied biases. We account for this by monitoring the drain current and subtracting the ohmic drops across the source and drain resistances. Also due to the ac negative feedback (see inset of Fig. 8 for equivalent circuit) of the source resistance, the intrinsic $g_{\text{ks}}$ has to be extracted from the measured quantity $g_{\text{km}}$ by

$$\frac{1}{g_{\text{ks}}} = (1 + gm\tau_s) \left( \frac{1}{g_{\text{km}}} - \frac{1}{R_T} \right)$$

(8)

where $gm$ is the transconductance at the given intrinsic bias and is obtained by

$$gm = \frac{\beta_0}{1 + \beta_0(V_{\text{gs}} - V_T)} V_{\text{ds}}.$$  

(9)

Points in Fig. 8 show the intrinsic $g_{\text{ks}}$ against intrinsic $V_{\text{dc}}$ for the two devices at intrinsic $(V_{\text{gs}} - V_T) = 3$ V extracted from $g_{\text{km}}$, according to (8). Based on the gradual channel model for device in the linear region of operation, $g_{\text{ks}}$ at nonzero $V_{\text{dc}}$ is

$$g_{\text{ks}} = \frac{\beta_0}{1 + \beta_0(V_{\text{gs}} - V_T)} (V_{\text{gs}} - V_T - V_{\text{dc}}).$$

(10)
It accounts for the gate bias-induced mobility reduction but not drain bias effects. Since \( g_{nk} \) and \( \theta \) are known for each device, we can calculate the expected \( g_{nk} \). This is shown as dotted lines in Fig. 8 for the two devices. It is clear that for the shorter device even for the drain bias of 200 mV, the experimental \( g_{nk} \) is significantly lower than the calculated value at the same bias. For the longer channel device there is no observable difference between experimental and calculated data. The observed reduction for short device is clearly due to those drain bias-induced effects referred to above but not modeled in (10). This indicates that small-signal \( g_{nk} \) can be used to determine those SPICE parameters used to model drain bias-induced effects before and after saturation. This is currently being investigated.

V. CONCLUSION

We have proposed and demonstrated a new and yet simple method for the simultaneous extraction of the threshold voltage, gain factor, gate bias mobility lowering factor, and source/drain series resistance from the measurement of small-signal source-drain conductance of a single MOSFET. When the measurement is carried out for devices with different drawn lengths, it is possible to extract the effective channel lengths and the inversion layer mobility. Results obtained by this extraction procedure compare well with those determined by existing measurement methods. The main advantage of the method is the simplicity and accuracy of the measurement as well as the number of parameters that can be extracted from a single measurement.

By using small ac signal and avoiding any dc drain bias, the measurement method has eliminated the influence of drain bias on the extraction of these parameters that model gate field effects. The method should be applicable to sub-0.1-\( \mu \)m devices where the channel electrical properties are more sensitive to the presence of any drain bias. The method should also be directly applicable to SOI MOSFETs as the measurement deals only with the inversion layer independent of the presence or absence of electrical contact to the substrate layer.

We have also demonstrated that small-signal source-drain conductance is sensitive to the effects of small changes in dc drain bias and therefore would be a good candidate for use to extract SPICE parameters modeling the effects of drain bias.

REFERENCES


Y. T. Yeow (M’76–SM’91) received the B.E. (Hons) degree from the University of Canterbury, Canterbury, New Zealand, the M.Sc. degree from University of Manchester, Manchester, U.K., and Ph.D. degree from University of Southampton, Southampton, U.K., 1975.

He is currently an Associate Professor in the School of Computer Science and Electrical Engineering, The University of Queensland, Australia. His teaching and research interests are in semiconductor device physics, electrical characterization, and numerical modeling.

Z. Q. Yao (S’94–M’95), photograph and biography not available at the time of publication.