Electrical Properties of MOCVD HfO_2 Dielectric Layers With Polysilicon Gate Electrodes for CMOS Applications

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Abstract

Electrical properties of MOS capacitors using MOCVD HfO_2 as gate dielectric have been investigated. A 900 °C 1s activation anneal of Ph-doped 680 °C-RTCVD demonstrated a good compatibility with high-k layers. The best MOS capacitor is obtained with EOT=1.93 nm and Jg=1.6E-04 A/cm^2 at $|V_{FB}-1|$ which is > 2 orders of magnitude lower than SiO_2 with Poly-Si gate. A minimal degradation of leakage current after 900 °C activation anneal and low effect of temperature dependence reveal the thermal stability of MOCVD HfO_2 gate stack. Nevertheless, upon 1000 °C activation anneal only the LPCVD poly resulted in working MOS capacitor. The found leakage current was 2 order of magnitude higher compared to a 900 °C activation anneal.

Keywords

MOCVD HfO_2, RTCVD Poly, LPCVD Poly, activation anneal

1. Introduction

To achieve high performance CMOS, the gate dielectric has to be continually scaled down. Beyond the 0.1 µm technology node, ultra thin SiO_2 layers of less than 10 Å thick exhibit significant leakage current densities (>1A/cm^2). Several high-k materials are being considered as a replacement for SiO_2 and SiON gate dielectrics [1,2]. In term of CMOS applications, HfO_2 is the high k material showing a good compatibility with polysilicon gate process [3]. In this paper, the considered gate stack Ph-doped-poly/HfO_2/RTO is investigated. MOS capacitors are used to study the electrical properties of the deposited stacks. Effect of post deposition anneals (PDA) at 600-1000 °C on devices quality is discussed. Thermal stability of MOCVD HfO_2 is studied by monitoring the changes of C-V and I-V as function of different activation anneals. The compatibility of RTCVD or LPCVD polysilicon with MOCVD HfO_2 is also discussed.

2. Experiment

A 1 nm RTO layer was grown on low B-doped Si (100) substrates after a 30s 2% HF-dip. The HfO_2 layers were deposited using Tetrakis Diethylamido Hafnium (TDEAH) in an Applied Materials MOCVD (Metal Organic Chemical Vapor Deposition) chamber. The total gate stack (HfO_2 + RTO) has a nominal thickness of 5 nm. The HfO_2/RTO stacks received a thin capping layer before the deposition of 100 nm phosphorous doped polysilicon in RTCVD-600/680°C and LPCVD-600°C systems. For convenience, HfO_2 + thin capping layer will be referred to HfO_2. Table 1 summarizes process conditions for all samples made. Activation anneals were done in N_2 at 900 and 1000°C for 1 sec in a Rapid Thermal Processing (RTP) system. MOS capacitors were used to evaluate HFC-V (100 MHz) and I-V. From C-V measurements, the Equivalent Oxide Thickness (EOT) is extracted using a simulation program considering quantum mechanical and polysilicon depletion effects.

Process flow	Parameter	W 1	A 2	F 3	E 4	R 5	S 6	7	8	9
Clean	Hf-dip 2%, 30s	x	x	x	x	x	x	x	x	x
SiO_2	800 °C, O_2	x	x	x	x	x	x	x	x	x
HfO_2	485 °C, TDEAH	x	x	x	x	x	x	x	x	x
PDA (1)	600 °C, O_2, 60s		x			x			x	
PDA (2)	1000 °C, O_2, 1s						x			
RTCVD	600 °C, SiH_4, PH_3	x						x	x	
RTCVD	680 °C, SiH_4, PH_3		x		x	x	x			
LPCVD	600 °C, SiH_4, PH_3			x						x

Table1: Summary of process conditions

3. Results and discussion

3.1 Effect of RTCVD Polysilicon temperature on device quality

The compatibility of HfO_2 gate stack with polysilicon has been reported in [4,5]. In this section, gate stack HfO_2/RTO capped by 600-680°C temperature of in-situ doped RTCVD polysilicon is studied. After activation anneal at 900°C for 1s, similar C-V characteristics are observed (Figure1).

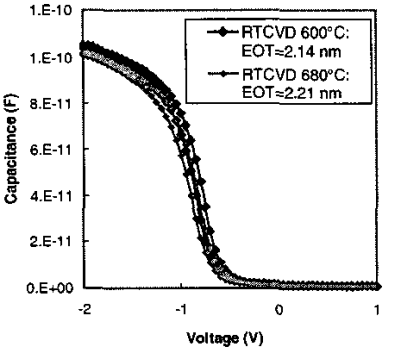

Figure 1: 600 and 680°C RTCVD poly comparison on HfO_2/RTO gate stack. C-V measurements performed at 25°C after activation anneal (900°C, N_2, 1s).

We also noted an insignificant difference in term of found EOTs (2.14 and 2.21 nm for 600 and 680°C, respectively). For the considered gate stacks, increasing the temperature measurement does not also impact significantly the C-V characteristics (Figure 2). Similar behavior was observed with RTCVD 680°C.

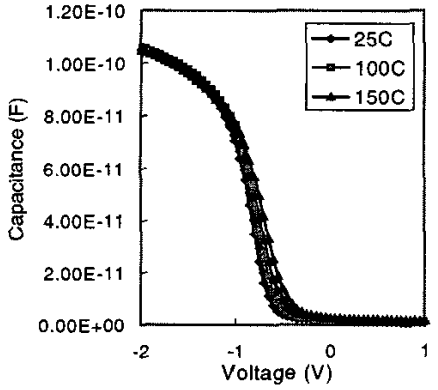

Figure 2: Impact of temperature measurement on C-V characteristics with 600 °C-RTCVD and activation anneal performed at 900 °C in N_2 ambient for 1s.

In Figure 3, we have plotted the temperature dependence of leakage current versus EOT for 600-680 °C RTCVD poly. Those results show clearly that for the considered gate stacks HfO_2/RTO (without PDA), 600°C RTCVD capping electrode is less good compared to 680°C one. By focusing to 680°C RTCVD, we noted a few effects on leakage current and EOT change for as-deposited layers with temperature dependence (25-150°C). However, after RTA at 900°C we noted a significant increase of leakage current by 2 orders of magnitude for sample measured at 150°C compared to 25 °C and 100 °C. This increase can be related to MOCVD HfO_2 thermal stability. Nevertheless, by using HfO_2/RTO gate stack (without a PDA) with an electrode of in-situ Ph-doped 680°C-RTCVD, we have achieved EOT=2.11 nm with Jg=1.8E-04 A/cm^2 at |Vfb-1|.

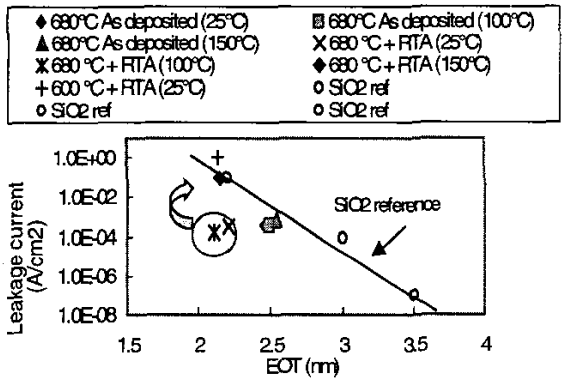

Figure 3: Leakage current at $|V_{FB}-1|$ versus EOT of 600-680 °C RTCVD Poly. Temperature dependence of those parameters from 25 to 150 °C is observed.

It is found that post deposition anneal is very effective to improve the MOCVD high k gate dielectrics quality in term of stability and leakage reduction [6]. 2 different conditions of PDA were applied to HfO_2/RTO gate stack prior to Ph-doped 680°C-RTCVD poly deposition.

Figure 4 shows the C-V characteristics of high k stack with a PDA at 600°C, 60s in O_2 ambient for 60s. Capacitance can be measured without gate electrode activation but the found EOT=2.36 nm is higher than sample with gate electrode annealed at 900°C, 1s (EOT=1.93 nm). Table 2 summarizes our electrical results including the temperature-dependency of EOT, V_{FB}, Q_f. By using those PDA conditions, the 25-150°C range of temperature measurement does not change significantly the EOT before and after gate activation anneal. In addition, a few temperature dependence of I-V characteristics observed (Figure 5), indicates that the fixed charge density is not critical in conduction mechanism.

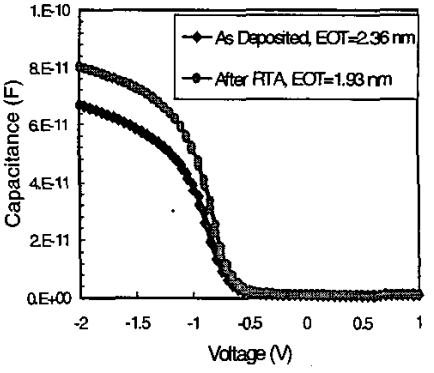

Figure 4: C-V of MOCVD HfO_2 with 600 °C in O_2 ambient for 60s capped by 100 nm 600 °C-RTCVD Poly.

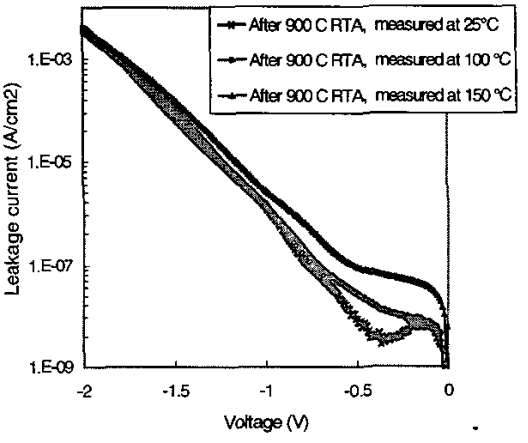

Figure 5: I-V of MOCVD HfO_2 (with 600 °C PDA) and 100 nm 680 °C-RTCVD Poly.

Sample	T (°C)	EOT (nm)	VFB (mV)	Qf(Cm^{-2})
As deposited (1)	25	2.46	-638	1.04E+11
As deposited (2)	100	2.49	-563	2.20E+11
As deposited (3)	150	2.54	-535	3.34E+11
900°C, 1s N2 (4)	25	2.21	-693	1.58E+11
900°C, 1s N2 (5)	100	2.11	-598	2.80E+11
900°C, 1s N2 (6)	150	2.15	-558	4.50E+11

Table 2: Summary of electrical results of investigated HfO_2-based stacks with 600 °C 60s O_2 PDA and 100 nm RTCVD Poly.

The temperature dependence of leakage current before and after 900°C anneal are shown in Figure 6. We noted an increase of Jg by ~ factor of 2 between 25 and 150°C for samples none-annealed. On the other hand, we observed an improvement of Jg with the increase of temperature, especially at 150°C (Jg =1.6E-04 A/cm^2 at |Vfb-1|). Consequently, not only PDA performed prior to ph-doped 680°C-RTCVD poly reduces EOT by ~3Å. In addition, RTO SiO_2 amorphous interfacial layer might be a barrier against current paths.

Upon 900 °C annealing, other PDA conditions at high temperature (1000 °C) in O_2 ambient for 1s have been explored. In Figure 7, we plotted an EOT comparison between both PDAs. A 1000°C PDA decreases the leakage current by 1 order of magnitude but this improvement comes with an increase of ~ 6Å EOT, most likely due to oxidation of the lower interface.

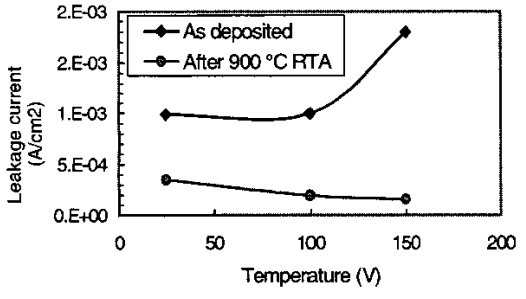

Figure 6: Temperature dependence of leakage current of 680 °C Poly-Si/HfO_2/RTO/Si structure (with 600 °C PDA).

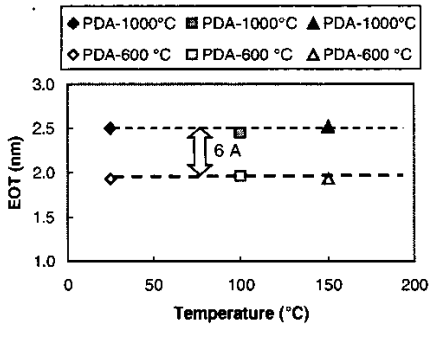

Figure 7: Impact of post deposition anneal on extracted EOT of sample capped with 100 nm 680 °C-RTCVD poly (900 °C activation anneal).

3.2 Characteristics of RTCVD and LPCVD gate electrodes with MOCVD HfO_2

Since the optimum poly process is deciding for MOS capacitors performance, we have explored 2 different techniques. Figures 8 and 9 show I-V and C-V characteristics, respectively, of an identical HfO_2/RTO gate stack capped with Ph-doped 600°C-LPCVD poly. These samples received no PDA prior to gate electrode deposition. After a 900°C, 1s N2 activation anneal, the extracted EOT is higher of ~ 3 Å compared to 600°C-RTCVD with a very low leakage (Jg=3.8 E-06 A/cm^2 at |Vfb-1|). Except the increase of EOT, the LPCVD system is the best technique for leakage reduction, at 600 °C. In the literature similar behavior has been observed implying growth of interfacial layer of HfO_2/Poly-Si, mostly with deposition temperature above 580°C [7,8]. However, increasing RTCVD poly process temperature up to 680°C yields to EOT reduction as well as leakage current. Overall, the best result of MOS capacitors is obtained with EOT=1.93 nm and Jg=1.6E-04 A/cm^2 at |Vfb-1| (discussed above).

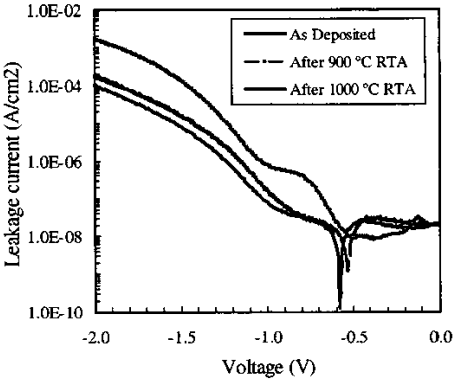

Figure 8: I-V of MOCVD HfO_2 (without PDA) and capped with 100 nm 600 °C-LPCVD Poly.

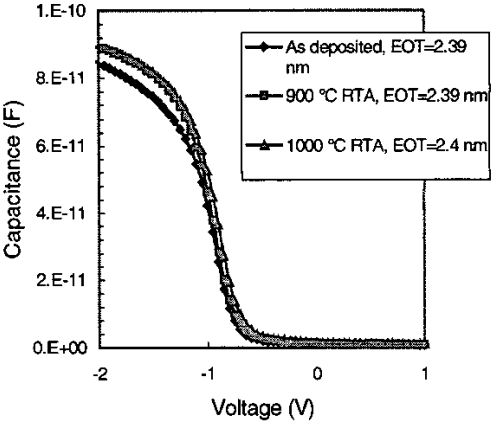

Figure 9: C-V of MOCVD HfO_2 (without PDA) capped with 100 nm 600-LPCVD Poly.

Thermal stability of MOCVD HfO_2 with poly using both deposition techniques is examined by increasing activation anneal temperature (Figure 8-9). Only samples with LPCVD do survive a 1000 °C annealing, although the leakage current increases by 1 order of magnitude compared to a 900 °C one.

Cross-section Transmission Electron Microscope (TEM) pictures of Poly-Si/ High k stack/Silicon structures are shown in Figures 10-12. As deposited layer (without PDA) illustrates a good uniformity and smoothness of gate dielectric/RTCVD poly as well as gate dielectric/Silicon interfaces (Figure 10). A bright contrast layer (~ 1 nm) observed at lower interface is assumed to be SiO_2. About 4 nm of dark contrast indicates high k stack. A slight grey contrast (upper interface between Poly-Si/HfO_2), about 2.5 nm is observed. The nature of this interfacial layer is not clear at the moment. Several hypothesis are advanced such as gate depletion caused by deficiency of phosphorous dopant, interaction between Si and HfO_2 during gate electrode deposition, etc. After 1000°C 1s N_2 activation anneal we did not observed a significant change in term of thickness, maybe related to TEM resolution. However, we noted some defects particularly at the upper interface (Figure 11). In fact, the 900 °C sample (Figure 12) exhibited a clearly defined and distinctive top interfacial layer when compared to 1000 °C sample [2]. Upper interface appeared to be rough. It is also reported that crystallization of metal oxide film deteriorates insulating properties [9] but with the cross-section TEM (Figure 11) of this sample it is hard to conclude concerning its crystallography.

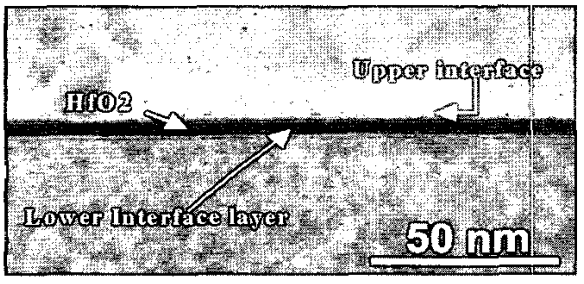

Figure 10: Cross-sectional TEM view of Poly-Si/HfO_2/RTO/Si as deposited.

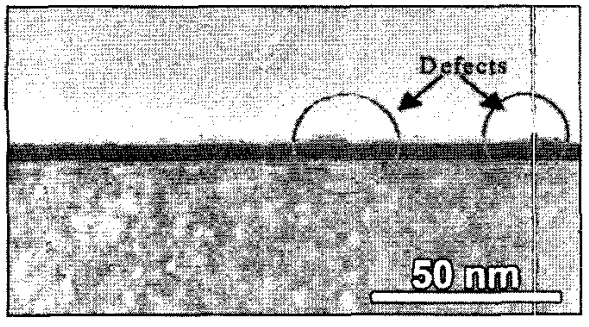

Figure 11: Cross-sectional TEM view of RTCVD Poly/HfO_2/RTO/Si after 1000 °C 1s N_2 activation anneal.

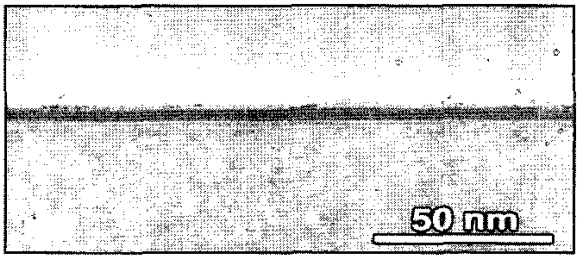

Figure 12: Cross-sectional TEM view of 680°C-RTCVD Poly-Si/HfO_2/RTO/Si after 900 °C 1s N_2 activation anneal.

Conclusion

In this paper, we have demonstrated the compatibility of MOCVD HfO_2 (+ thin capping layer) with in-situ Ph-doped RTCVD and in-situ Ph-doped LPCVD poly. At low process temperature (600 °C), LPCVD technique is better than RTCVD for gate electrode deposition in terms of poly compatibility with MOCVD high k gate stack. However, our results show that the potential reduction of poly depletion is much lower with the RTCVD compared to LPCVD. After 900 °C 1s N_2 activation anneal, 680°C-RTCVD technique provides the best gate electrode for EOT and leakage reductions. The lowest found EOT was 1.93 nm for HfO_2 deposited on 1 nm RTO followed by a PDA at 600 °C O_2 60s. Post deposition anneal performed at high temperature (1000 °C) improve leakage current by 1 order of magnitude but with ~ 6Å EOT increase. Up to 1000 °C layers capped by RTCVD poly exhibited a drastic leakage current increase might be related to significant modification of upper interface as shown by TEM. Optimized RTCVD poly process must be selected for high activation anneal temperature. A suitable barrier might be also required at both the interfaces with MOCVD high k gate stack.

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