MOS Capacitor on 4H–SiC as a Nonvolatile Memory Element

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***Abstract*—Nonvolatile memory characteristics of MOS capacitors are presented in this letter. The MOS capacitors have been fabricated on N-type 4H SiC substrate with nitrided oxide–semiconductor interface. The charge-retention time is in the order of 4.6×10^9 years, as determined by thermally activated (275–355 °C) capacitance–transient measurements and extrapolation to room temperature. The estimated activation energy of the charge-generation processes is 1.6 eV. The results and the analysis presented in this letter demonstrate that 4H SiC MOS capacitors can be used as a memory element in nonvolatile RAMs.**

***Index Terms*—Carrier generation, charge-retention time, MOS capacitor, nitridation, nonvolatile memory, random-access memory (RAM).**

I. Introduction

CURRENTLY, the term nonvolatile memory is associated with a variety of so-called read-only memory (ROM) elements. These devices can only withstand about 10^6–10^7 charging/discharging cycles, with too long charging/discharging times to allow their use for random-access memory (RAM) applications [1]–[3]. The charge storage in these devices is achieved by trapping the charge in a deep potential well, created by energy-band discontinuity of two materials (typically, semiconductor and oxide). As the energy-band discontinuity does not change with voltage applied, the charging/discharging is achieved by charge tunneling through very thin material (typically oxide) creating the "walls" of the potential well. This is a slow process and one with limited charging/discharging cycles.

In MOS capacitors, the surface band bending due to gate voltage also creates a potential well. This allows the MOS capacitor to be used as a memory element, which is the case in modern dynamic RAMs. In silicon, however, the generation and recombination of minority carriers are relatively fast, so the memory has to be refreshed. Silicon carbide (SiC) is a wide band-gap material, and the generation/recombination rates are orders of magnitude lower. The generation rate is directly proportional to the intrinsic-carrier concentration [4], which is 10^{10} cm^{-3} in silicon and in the order of 10^{-7} cm^{-3} in 4H SiC. Therefore, the time needed to generate minority carriers in 4H SiC should be 17 orders of magnitude longer than in Si [5], meaning that a MOS capacitor could operate as a nonvolatile RAM element with access characteristics of silicon dynamic RAM and retention characteristics of ROM.

Gardner *et al.* [6] and Xie *et al.* [7] proposed a 6H–SiC memory element, where the potential well was created by n-p-n structure. They reported retention time of 10^{14} s (3×10^6 years) at room temperature, as extrapolated from high-temperature measurements. They also found that the generation and recombination rates depended very strongly on the quality of the surface passivation at the junction terminations. The reason for that was poor quality of the passivating oxide–SiC interface, in particular, the existence of large density of defects related to carbon accumulation at the interface. As a consequence, the generation assisted by these defects or leakage through the gate oxide was so high that no charge retention data have been reported for MOS capacitors on SiC.

Recently, we have shown that the interface carbon can be removed and that the SiO_2–SiC interface can be passivated by growing the oxide (or annealing pregrown oxide) in NO or N_2O ambients [8]–[10]. Utilizing this high-quality interface, we report in this letter nonvolatile memory characteristics of MOS capacitors.

II. Experiments Details

Si-faced, n-type 4H–SiC wafer with 3 μm thick epilayer (doping level of 1.8×10^{16} cm^{-3}) oriented 8° off (0001) direction was purchased from CREE Research and used to fabricate the MOS capacitors. The wafer was first cleaned in a mixture of H_2SO_4 and H_2O_2, followed by an RCA clean. Immediately prior to oxidation, the wafer was dipped in HF (1%) for 1 min. The oxide was grown in 10% N_2O gas at 1300 °C for 270 min. The gas flow through the quartz tube was kept at one standard liter per minute. After the oxide growth, the samples were cooled down to 800 °C in N_2 at approximately 300 °C/h (this was the only post-oxidation treatment/annealing). Subsequently, metallization and photolithography were performed to create the MOS capacitors. The oxide thickness was in the range from 23–28 nm. The characterization was performed by capacitance–transient (C–t) measurements, using an HP4284A LCR meter. In order to accelerate the thermal generation and recombination processes, the measurements were performed at temperatures up to 355 °C. For fast generation of minority carriers, the samples were exposed to UV light. Note that, in actual application, no exposure to UV light would be necessary: as in Si DRAMs, a select MOSFET would be connected to the MOS capacitor to enable its charging/discharging process.

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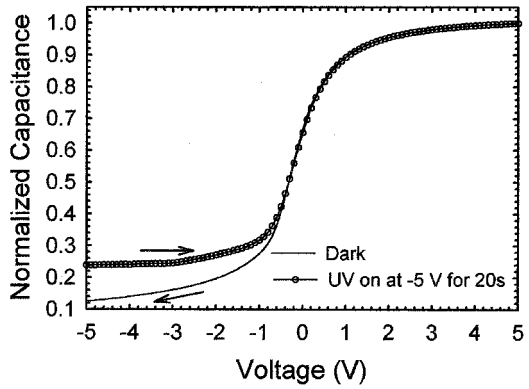

Fig. 1. Typical C–V curves before and after illumination with UV light. Arrows indicate DC sweeping directions. Gate-oxide thickness is 27 nm.

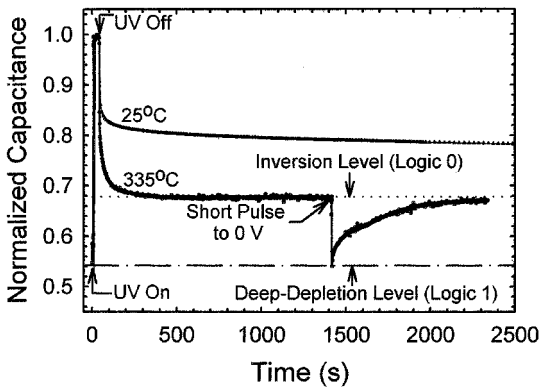

Fig. 2. High-temperature (335 °C) and room temperature (25 °C) C–t plot, illustrating the memory effect and demonstrating that the retention time is determined by carrier generation causing the capacitance increase from the deep-depletion level toward the inversion level.

III. Results and Discussion

Typical capacitance–voltage (C–V) curves, normalized by the accumulation capacitance, of MOS capacitor with gate-oxide thickness of 27 nm are shown in Fig. 1. The C–V curve before illumination is measured by sweeping the voltage from accumulation to deep depletion. Following this, the MOS capacitor is biased in deep depletion (-5 V) and illuminated by UV light, which generates minority carriers in excess of the thermal-equilibrium concentration. Immediately after switching off the light, positive-bias sweep is initiated resulting with a constant capacitance, well above the inversion level. This steady-state capacitance corresponds to "threshold" surface potential of about -0.7 V: the reduction of the gate voltage due to the bias sweep does not reduce the surface potential as the excess minority carriers are injected into the substrate. As a result, the depletion-layer width and the measured capacitance are constant. An important conclusion from this observation is that the MOS capacitor could be charged to the theoretical maximum of the minority-carrier density, corresponding to the surface potential of about -0.7 V.

Typical data from the high temperature (335 °C) C–t measurements are presented in Fig. 2. It can be seen that generation-recombination balance is reached in the first 20 s under the illumination, causing constant capacitance in time. When the UV light is switched off, the generation rate drops to nearly zero, so that the high injection and recombination rates cause relatively fast capacitance decay. However, as the density of minority carriers is reduced, the surface potential shifts from about -0.7 V toward the original -5 V so that the minority carriers can no longer be injected into the substrate. From that point on, the capacitance change slows down, following exponential decay in time toward the inversion level. The state corresponding to the inversion level can be defined as logic 0 state. When a short pulse to 0 V is applied to the gate of MOS capacitors, the minority carriers are quickly discharged through recombination with majority carriers, and the capacitance drops to its deep-depletion level (the application of deep-depletion pulse was always used to confirm that the capacitor can instantly be discharged to the deep-depletion level). We define the deep-depletion state, in which the minority carrier concentration is negligible, as logic 1 state. At elevated temperatures, the generation of minority carriers is accelerated, leading to measurable increase of the capacitance from the deep-depletion level toward the inversion level. The capacitance increases exponentially, so the time constant is defined as the retention time.

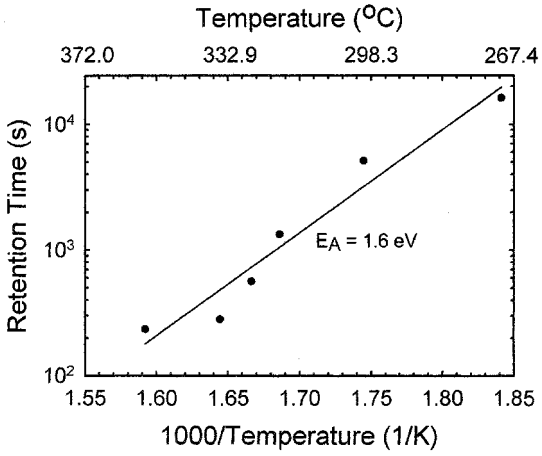

Fig. 3. Retention times at different temperatures.

Fig. 3 presents the MOS capacitor retention times for different ambient temperatures. The activation energy, determined from the slope, is 1.6 eV. This value is approximately equal to the half of the energy gap, indicating that the generation rate follows the same temperature dependence as the intrinsic carrier concentration. Extrapolation of the retention time to room temperature gives the value of 1.5×10^{17} s (4.6×10^9 years). Given that the intrinsic-carrier concentration of 4H–SiC is about 17 orders of magnitude lower compared to silicon, this retention time corresponds to 1.5 s in silicon, clearly indicating that the quality of the nitrided SiO_2–SiC interface (in terms of carrier-generation rate) is comparable to the SiO_2–Si interface. Comparing with the retention time (10^{14} s or 3×10^6 years) obtained by Xie *et al.* [7], it is also obvious that dramatic improvement in the quality of SiC–oxide interface is achieved. Consequently, the minority carrier generation through the SiO_2–SiC interface is reduced so much that the retention time of the MOS capacitor itself is three orders of magnitude longer. This is long enough time to enable the MOS capacitor to be used as a nonvolatile RAM element, avoiding complex technology associated with the memory element based on n-p-n structures.

IV. Conclusions

In this letter, we have reported the results on nonvolatile memory characteristics of N-type 4H–SiC MOS capacitors with nitrided SiO_2–SiC interface. The charge-retention time (extrapolated to room temperature) and the activation energy are 1.5×10^{17} s (4.6×10^9 years) and 1.6 eV, respectively. These values are fully consistent with the theoretically expected values for 4H–SiC. The results presented in this letter demonstrate that 4H–SiC MOS capacitors can be used as nonvolatile RAM elements.

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