

Si Surface Preparation for Heteroepitaxial Growth of SiC Using in situ Oxidation

Li Wang^{1,a*}, Sima Dimitrijević^{1,b}, Alan Iacopi^{1,c}, Leonie Hold^{1,d}, Glenn Walker^{1,e},
Jessica Chai^{1,f}, David Massoubre^{1,g}

¹Queensland Micro- and Nanotechnology Centre, Griffith University, Nathan, Qld, 4111, Australia

^al.wang@griffith.edu.au, ^bs.dimitrijevic@griffith.edu.au, ^ca.iacopi@griffith.edu.au,
^dl.hold@griffith.edu.au, ^eglenn.walker@griffith.edu.au, ^fj.chai@griffith.edu.au,
^gd.massoubre@griffith.edu.au,

Keywords: Silicon surface cleaning, chemical vapour deposition, silicon carbide, epitaxial growth, off-axis.

Abstract. To achieve high quality SiC growth on Si substrate, it is essential to get a smooth Si surface without forming SiC and graphitic islands during the surface cleaning and before the carbonisation process. In this paper, a novel in-situ surface cleaning method designed for the heteroepitaxial growth of SiC on Si substrate is developed using a custom-made low-pressure chemical vapour deposition reactor. The results indicate that the combination of ramping in oxygen and subsequent flowing of SiH₄ avoids the contamination of Si, enables the oxide layer to be removed smoothly, and subsequently creates a smooth Si surface with regular atomic steps. SiC grown on off-axis Si has better crystallinity and significantly smaller roughness than that grown on on-axis Si.

Introduction

Silicon surface preparation is extremely important for epitaxial film growth and other-related semiconductor processing technology. The cleaning of oxide includes ex-situ and in-situ cleaning steps. Hydrofluoric acid is widely used as an ex-situ method to remove the native oxide layer, however, a fresh Si surface easily get oxidized and contaminated by oxygen and carbon during the temperature ramping steps. In order to maintain the smoothness of the fresh Si surface and protect it from contamination, a protective oxide layer can be grown using chemical solutions before subsequent processing [1], thus, an in-situ oxide removal process is still needed to get fresh Si surface for any epitaxial processes.

The in-situ thermal desorption of the thin silicon dioxide layer starts to occur at high temperatures (as a function of oxygen pressure) [2]. However, this thermal desorption process is inhomogeneous/anisotropic: roughening and faceting of the Si surface were observed [1, 2], worse on Si(111) than Si(100). To assist the removal of oxide layer and keep a smooth Si surface, hydrogen is usually employed as atomic hydrogen can passivate the Si surface by forming Si–H bonds. Since stable Si–H bond can only exist when temperature is below 400°C [3], no passivation effect can be achieved beyond this temperature. However, with the aid of mobilizing Si atoms, high temperature annealing under high pressure hydrogen (>10⁴ Pa) is still widely employed during the Si surface cleaning process [4], possibly because that the dynamical balance between formation and breakage of Si–H bonds help to maintain the smoothness of the Si surface. High temperature annealing under high vacuum and a rapid ramp to high temperature are also used to achieve the desirable smoothness of the clean Si surface, however, when there are contamination sources present, annealing under high vacuum could not avoid the chemical reaction between the contamination source and the Si substrate. A rapid ramp to high temperature is also not practical for reactors that have a slow heating-up rate.

In this investigation, the employed custom-made low-pressure chemical vapour deposition (LPCVD) reactor has an upper pressure limit of ~100 Pa and temperature limit of 1300°C. The low pressure processing regime enables, a conformal SiC deposition on large-diameter Si substrates (≤300 mm) by using alternating supply epitaxy (ASE) at relatively low deposition temperature [5]. It enables depositions with void-free SiC/Si interface and precise thickness control: thickness

adjustment at nm scale and non-uniformity less than 1 %. These fine controls are crucial for the fabrication of complex structures, such as SiC/AlN distributed Bragg reflector (DBR), which requires a good control of layer thickness in order to enhance the reflectance [6], making it practical for the retention of Si substrate for the low-cost GaN/Si light-emitting diode manufacture. For the growth of 3C-SiC on Si substrate, a carbon-containing gas has to be employed, which results in potential carbon-based contamination in the reactor. Therefore, in this paper, a unique in-situ surface cleaning process is developed for Si(111) wafers; the crystallinity and surface roughness of SiC grown at 1200°C on cleaned Si are investigated.

Experiments

The in-situ surface cleaning was performed on both on-axis (off-cut angle $<0.5^\circ$) and off-axis (off-cut angle of $3.5 \pm 0.5^\circ$ towards [110]) 150-mm Si(111) substrates (both are p-type doped with resistivity in the range of $1\sim 10 \Omega \cdot \text{cm}$) using a custom-made LPCVD reactor. Si wafers were loaded into the reactor at 600°C as received (without pre-treatment). The temperature was ramped up at a rate of 5°C/min from 600 to 1000°C either in vacuum or under oxygen (flow rate: 100 sccm, pressure 95 Pa). The native oxide formed on the Si substrate surface was removed using low pressure SiH₄ at 1000/1200°C (<0.1 Pa) to ensure a smooth Si surface. The surface morphology of Si was observed using scanning electron microscopy (SEM, model: JEOL JSM-6510LV) and atomic force microscopy (AFM, model: Park NX20) under non-contact mode. A carbonisation step was employed to convert the Si surface into SiC layers before the subsequent SiC growth (at 1200°C using alternating supply epitaxy), the crystallinity, surface morphology and roughness were characterised using AFM and PANalytical Empyrean x-ray diffractometry (XRD).

Results and discussions

Naturally grown oxide layer might act as an effective barrier for further reaction between carbon and Si substrate. However, once this oxide layer starts to decompose thermally during the temperature ramping (in vacuum, pressure <0.1 Pa) from 600 to 1000°C, Si surface can roughen and chemical reactions between contamination sources and Si can occur, as shown by SEM top-view images in Fig. 1 for both on-axis and off-axis Si(111) wafers, The Si surface is quite rough (the peak to valley height is around 127.78 nm) with irregular saw-teeth shaped corrugated terraces, particles/islands were also seen pinned mostly around the step edges. Therefore, to get a smooth Si

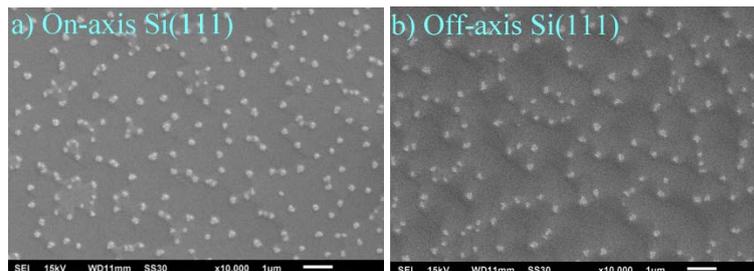


Fig. 1. SEM top-view images of on-axis and off-axis Si(111) wafers when temperature was ramped from 600 to 1000°C in vacuum (pressure <0.1 Pa). a) Morphology of on-axis Si, b) Morphology of off-axis Si.

surface, it is necessary to remove the oxide layer in a well-controlled manner rather than leave it thermally decomposed in vacuum. To achieve this, a high pressure of oxygen (~ 95 Pa) was used during the temperature ramping-up step (from 600 to 1000°C) to retain the oxide layer and to react with carbon-based residues in the reactor. Upon reaching 1000°C, an isothermal anneal under oxygen was performed for 1.5 h to minimise the risk of carbon-based contamination of the silicon surface. The oxide formed on the Si substrate surface was then removed using low pressure SiH₄ (1.0 sccm) at 1000°C or 1200°C to ensure a smooth Si surface (SiH₄ reacts with oxide to form volatile monoxide). Following the removal of oxide, the continued SiH₄ flow results in a deposition of a fresh layer of Si on the activated Si substrate, the process diagram is shown in Fig. 2. The AFM

images of the Si surface prepared in this way are shown in Fig. 3, where regular step-like features were observed on both on-axis and off-axis wafers. The root mean square (RMS) roughness for on-axis Si is around 0.17 (at 1000°C, Fig. 3a)) and 0.13 nm (at 1200°C, Fig. 3b)) over $1\ \mu\text{m} \times 1\ \mu\text{m}$ scan area, the terrace width ranges from ~ 155 to ~ 322 nm with an average step height of 0.31 nm [7], indicating that Si(111) surface is composed of steps with uniform step height of one monolayer. The calculated off-cut angle for the on-axis Si substrate is therefore less than 0.1° , and no obvious step-bunching phenomenon was observed. Tiny particulates were seen evenly populating on the on-axis Si wafer surface at 1000°C, comparatively, particle-free Si surface with regular surface steps was obtained by raising the temperature to 1200°C. The off-axis Si has a larger RMS roughness at 1.55 nm over $1\ \mu\text{m} \times 1\ \mu\text{m}$ scan area (shown in Fig. 3c) and d)) for Si wafers processed at both 1000°C and 1200°. Highly parallel steps, which are normal to the wafer primary flat, have been observed. The step density on off-axis wafer is twice as high as that on the on-axis wafer, with step spacing ranged from ~ 82 nm to ~ 117 nm and step height varied from 6.67 nm to 8.33 nm [7], indicating that step bunching occurred during the thermal treatment.

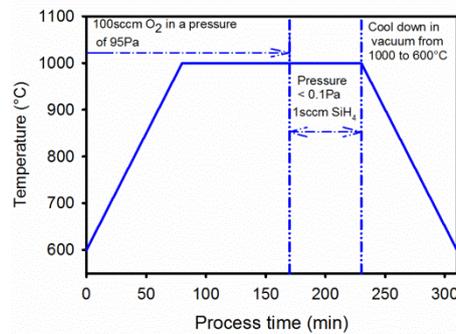


Fig. 2 Diagram of Si surface cleaning process.

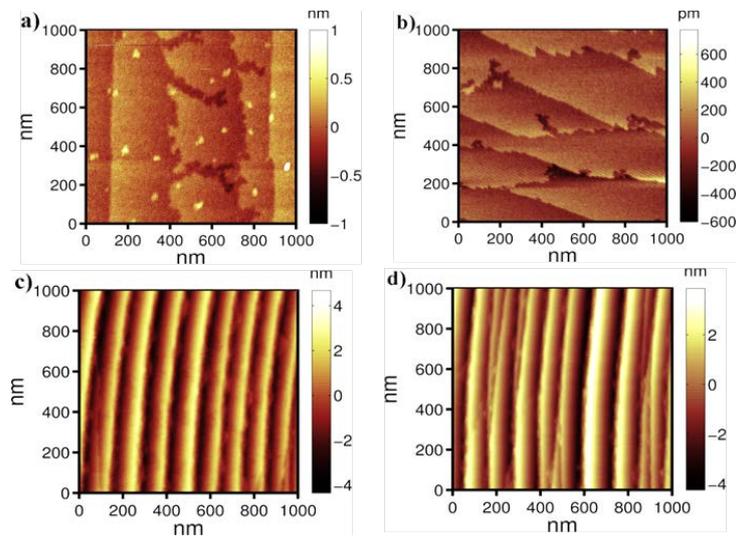


Fig. 3. Top-view AFM images of Si surface after in-situ cleaning: (a) on-axis Si prepared at 1000°C, RMS=0.17 nm, (b) on-axis Si prepared at 1200°C, RMS=0.13 nm (c) off-axis Si prepared at 1000°C, RMS=1.55 nm, and (d) off-axis Si prepared at 1200°C, RMS=1.55 nm. The scan area is $1\ \mu\text{m} \times 1\ \mu\text{m}$.

SiC film with a thickness around 558 ± 5 nm was deposited on the cleaned Si substrates, the RMS roughness from AFM measurement and FWHM of SiC(111) peak from XRD rocking curve scan are shown in Table 1. The top-view surface morphology from AFM scans is shown in Fig. 4. Triangular features were seen for SiC grown on on-axis Si, while dense line features in the direction parallel to the original Si surface steps were seen for SiC grown on off-axis Si, indicating a step-

controlled growth mode. As a result, the SiC grown on off-axis Si has better crystallinity (FWHM of $0.64\pm 0.03^\circ$) and smaller roughness (3.98 ± 0.2 nm). Both the on-axis and off-axis grown SiC have a slightly wider FWHM but smaller RMS roughness value compared to the SiC film grown by concurrent supply epitaxy [8].

Table 1 Properties of SiC films (thickness: 558 ± 5 nm) grown by ASE method at 1200°C .

SiC sample label	RMS roughness in a scan area of $5\ \mu\text{m} \times 5\ \mu\text{m}$ [nm]	FWHM of rocking curve scan of SiC(111) peak [$^\circ$]
SiC_on-axis	9.60 ± 0.4	0.78 ± 0.03
SiC_off-axis	3.98 ± 0.2	0.64 ± 0.03

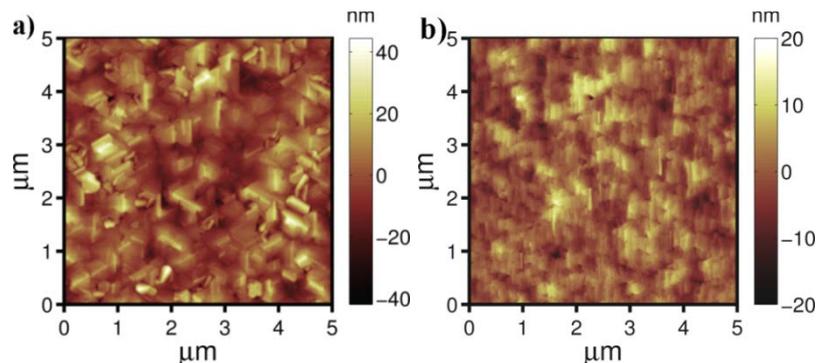


Fig. 4. Top-view AFM images of SiC (558 ± 5 nm) grown at 1200°C in a scan area of $5\ \mu\text{m} \times 5\ \mu\text{m}$: on (a) on-axis Si, (b) off-axis Si.

In summary, smooth Si surface with regular atomic steps was obtained on both on-axis and off-axis Si. The combination of ramping in oxygen and subsequent flowing of SiH_4 enables the oxide layer to be removed smoothly, carbon contamination is also avoided. The step density and height of a clean Si surface is dependent on the off-cut angle. The SiC film grown on off-axis Si has better crystallinity and smaller roughness due to the step-controlled growth compared to SiC grown on on-axis Si. This in-situ Si surface cleaning method is expected to be applicable to any reactors that are working under extremely low pressure range with/without potential contamination sources present in the reactor due to the previous deposition processes.

Acknowledgments

The SiC deposition, performed at Queensland Microtechnology Facility, Griffith University, Australia, was funded by SPTS Technologies and Smart Future Funds Research Partnerships Program Grant. This work was performed in part at the Queensland Node of the Australian National Fabrication Facility. The authors would like to thank Ms. Alanna Fernandes from Bluglass Ltd. Australia for performing high resolution XRD measurements.

References

- [1] A. Irajizad, N. Taghavinia, M. Ahadian, A. Mashaei, *Semicond. Sci. Technol.* **15** (2000) 160.
- [2] F. Smith, G. Ghidini, *J. Electrochem. Soc.* **129** (1982) 1300.
- [3] H. Hirayama, T. Tatsumi, *Appl. Phys. Lett.* **54** (1989) 1561.
- [4] K. Oda, Y. Kiyota, *J. Electrochem. Soc.* **143** (1996) 2361.
- [5] L. Wang, S. Dimitrijević, J.S. Han, A. Iacopi, L. Hold, P. Tanner, H.B. Harrison, *Thin Solid Films* **519** (2011) 6443.
- [6] D. Massoubre, R. Chu, L. Wang, J.D. Guo, J. Chai, G. Walker, L. Hold, A. Iacopi, 8th International Workshop on Nitride Semiconductors (IWN 2014).
- [7] L. Wang, A. Iacopi, S. Dimitrijević, G. Walker, A. Fernandes, L. Hold, J. Chai, *Thin Solid Films* **564** (2014) 39.
- [8] M. Katagiri, H. Fang, H. Miyake, K. Hiramatsu, H. Oku, H. Asamura, K. Kawamura, *Jpn. J. Appl. Phys.* **53** (2014) 05FL09.