A temperature independent effect of near-interface traps in 4H-SiC MOS capacitors

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Abstract. In this paper we report temperature independent near-interface traps (NITs) in the gate oxide of N-type MOS capacitors. The measurements were performed by a recently developed direct-measurement technique, which detected NITs with energy levels between 0.13 eV to 0.23 eV above the bottom of conduction band. These traps are also spatially localized close to the SiC surface, as evidenced by the fact that they are not observed at measurement frequencies below 6 MHz. The temperature independence indicates that this localized defect is different from the usually observed NITs whose density is increased by temperature-bias stress.

Introduction

Although SiC MOSFETs have been commercialized, they still suffer from performance issues mainly due to low channel-carrier mobility. The high density of defects at the interface of SiC and gate oxide is mostly responsible for the low channel-carrier mobility [1−3]. Capacitance and conductance measurements with MOS capacitors are commonly used to characterize the interface between SiC and the gate oxide. The area of interest is the strong-accumulation region of N-type SiC MOS capacitors, which is analogues to the strong-inversion region of SiC MOSFETs, because the energy levels of the active near-interface traps (NITs) are aligned to the conduction band due to the quantum confinement effect [1−3]. The conductance in accumulation is particularly sensitive to the specific calibration of the measurement equipment, as illustrated in Fig. 1. Performing careful calibration of an Agilent B1505A LCR meter, we were able to obtain the constant capacitance in strong-accumulation up to 5 MHz. However, the corresponding conductance in accumulation appears positive only at lower frequencies and shows large negative values at 5 MHz, as shown in Fig. 1. We assume that this issue was due to the sensitivity of LCR meter parameter extraction (C and G) to slight distortions in the measured sinusoidal signals. To check this assumption, we have recently performed and published direct measurements of the alternating current through the MOS capacitors in the strong-
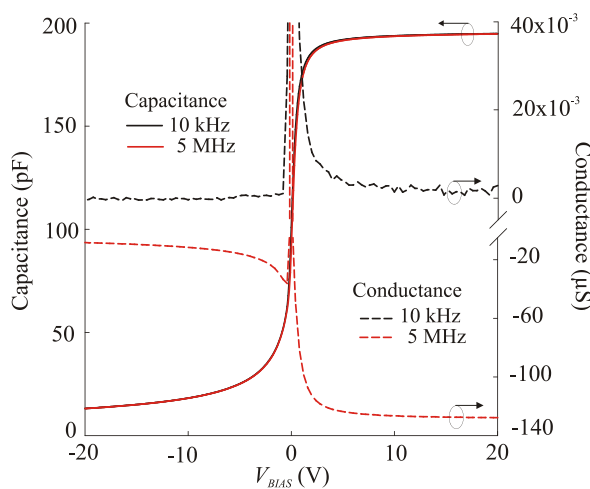

Fig. 1. Capacitance–voltage and conductance–voltage characteristics of a measured MOS capacitor at 10 kHz and 5 MHz. The capacitance is constant in strong-accumulation, however the corresponding conductance is *positive* at 10 kHz while showing large *negative* values at 5 MHz.

accumulation region [4]. The measurements identified a distortion in the sinusoidal current, which we assigned to near-interface traps (NITs) with energy levels between 0.13 eV and 0.23 eV above the bottom of the conduction band. Charging and discharging of NITs with energy levels above the bottom of the conduction band must occur by tunnelling, which is a temperature-independent mechanism [2–3]. However, it was found that high-temperature bias stress changes the density of these NITs [5–8], which Lelis *et al*. explained by temperature activation of defective bonds [9]. In this paper, we investigate the temperature dependence of the spatially and energetically localized NITs, which we identified by the recently published direct-measurement technique [4].

Experimental details

Silicon faced, N-type, 4H-SiC wafer with 10^{16} cm^{-3} nitrogen doped epitaxial layer of 5 µm was used to fabricate the MOS capacitors. The samples were cleaned by the standard Radio Corporation of America (RCA) procedure prior to oxidation. The gate oxides were grown at 1250°C for 1 hour in dry O$_2$ followed by a 1 hour anneal in nitric oxide at 1250°C. An oxide thickness of 45 nm was determined from the accumulation capacitance.

The measurements were performed by connecting the MOS capacitors (*C*) under test in series with an external resistor (*R*) of 120 Ω and applying sinusoidal voltage signal across the series connection of the external resistor and the MOS capacitors. Superimposed on the sinusoidal signal was a DC voltage to bias the capacitors in accumulation. Sinusoidal signals with frequencies from 10 kHz to 8 MHz, fixed amplitude of 500 mV, and the bias voltage (V_{BIAS}) ranging from 5 V to 20 V were used. The amplitude of 500 mV is chosen so to minimize noise while maintaining the signal below the value of the bias-voltage step. To perform high-temperature bias stress measurements, the MOS capacitors were stressed with 15 V for 12 hours at different temperatures. All the measurements before and after stress were performed at 25° C, 125° C and 175° C. Multiple capacitors were measured to ensure the repeatability of the results.

Results and discussion

Initially the measurements were performed at different temperatures without stressing the MOS capacitors. Figure 2 shows the typical measured current through the MOS capacitors, i_{C-meas} (coloured lines), at 7 MHz with different bias voltages and at different measurement temperatures before stress. Figure 2 also shows the current through a capacitor without NITs, i_C (black lines), which is calculated as: $i_C(t) = [v_{IN}(t) - v_C(t)]/R$ where $v_C(t)$ is the voltage across constant capacitor (*C*) in response to the measured input voltage $v_{IN}(t)$ [4]:

$$v_C(t) = \exp\left(-\frac{t}{RC}\right)\left[A_0 + \frac{1}{RC}\int_0^t v_{IN}(t_S)\exp\left(\frac{t_S}{RC}\right)dt_S\right]$$ (1)

In Eq. (1), t_S is the variable time within the integration interval ($0 \leq t_S \leq t$) and A_0 is the integration constant.

The current through the MOS capacitors was then measured after stressing the capacitors with 15 V for 12 hours at different temperatures. The measurements performed after stress showed no significant change in measured currents as compared to currents measured before stress.

The maximum difference between i_C and i_{C-meas} was observed at 7 MHz with 11 V bias voltage during the charging of the capacitor, which was essentially the same at all measured temperatures (25°C, 125°C and 175°C). The asymmetry between the charging and discharging currents is due to different charging and discharging times of the NITs.
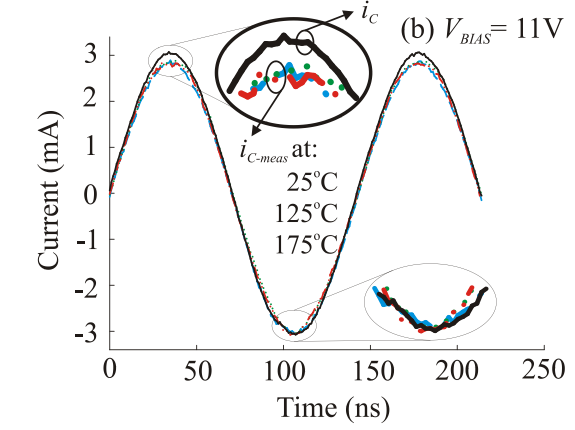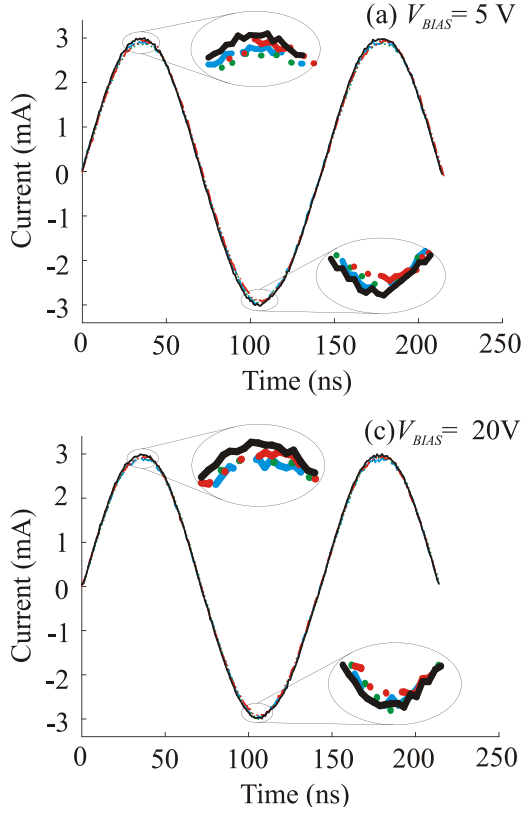
(a) V_{BIAS}= 5 V

(b) V_{BIAS}= 11V

i_C

i_{C-meas} at:
25°C
125°C
175°C

(c)V_{BIAS}= 20V

Fig. 2. The calculated current through a capacitor without NITs, i_C (black line), and the typical measured current through the MOS capacitor, i_{C-meas}, corresponding to different temperatures: 25°C (blue dash line), 125°C (green dotted line), and 175°C (red dash dot-dot line) at 7 MHz for (a) 5 V bias voltage, (b) 11 V bias voltage, and (c) 20 V bias voltage. There is no significant temperature dependence of the measured current.

Due to the quantum confinement effect the Fermi level (E_F) of the N-type MOS capacitor crosses the bottom of conduction band (E_C) when biased in strong-accumulation. The effect of the bias voltage observed in Fig. 2 can be presented in terms of conduction band and the energy location of the active NITs (E_{NIT}), as explained by Pande et al. [4].

The density of NITs (D_{NIT}) as a function of their energy location above the bottom of conduction band can be calculated from the following equation [4]:

$$D_{NIT} = \frac{1}{2kTqA} \int_{t_1}^{t_2} \Delta i_C(t)dt \qquad (2)$$

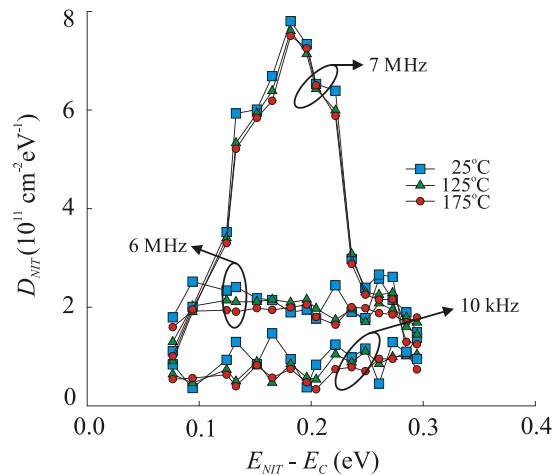In Eq. 2, $\Delta i_C = i_C - i_{C-meas}$, A is the capacitor area (500x500 µm^2), q is the electron charge, and t_1 and t_2 are the integration limits of the charging period of the capacitor.

The maximum D_{NIT} is found to be between 0.13 eV to 0.23 eV above the conduction band and it does not change with temperature, as shown in Fig. 3. The sharp increase in D_{NIT} demonstrates that the distribution of the NITs peak at a physical location very close to the SiC surface where tunnelling distances correspond to 7 MHz. This shows that the NITs are fast enough to allow the i_{C-meas} to follow the i_C up to 6 MHz and when a faster signal of 7 MHz is applied, the i_{C-meas} is unable to follow the i_C.

Fig. 3. Measured density of near-interface traps at different frequencies and temperatures.

As there were no changes observed in measured current after high-temperature bias stress as compared to before stress it is clear that the NITs identified here are different from NITs whose density is increased by temperature-

bias stress. Consequently, it is evident that the observed effect is temperature independent and can only be attributed to tunnelling between the NITs and the SiC surface.

Summary

In this paper, we have identified temperature independent NITs whose density peaks between 0.13 eV to 0.23 eV above the bottom of the conduction band. The NITs are active at measurement frequencies above 6 MHz, showing that the responsible defects is spatially localized close to the SiC surface. The observed temperature independence confirms that NITs trap and de-trap electrons by tunnelling and also demonstrates that this specific defect is not activated by temperature.

Acknowledgement

References

[1] R. Y. Khosa, E. Ö. Sveinbjörnsson, Conductance signal from near-interface traps in n-type 4H-SiC MOS capacitors under strong accumulation, Mater. Sci. Forum, 897 (2017), 147–150.

[2] H. A. Moghadam, S. Dimitrijev, J. Han, D. Haasmann, A. Aminbeidokhti, Transient-current method for measurement of active near-interface oxide traps in 4H-SiC MOS capacitors and MOSFETs, IEEE Trans. Electron Devices, 62 (2015) 2670–2674.

[3] D. Haasmann, S. Dimitrijev, Energy position of the active near-interface traps in metal–oxide–semiconductor field-effect transistors on 4H–SiC, Appl. Phys. Letters, 103 (2013) 113506-1–113506-3.

[4] P. Pande, S. Dimitrijev, D. Haasmann, H. A. Moghadam, P. Tanner, J. Han, Direct measurement of active near-interface traps in the strong-accumulation region of 4H-SiC MOS capacitors, IEEE J. Electron Devices Soc., 6 (2018) 468–474.

[5] H. A. Moghadam, S. Dimitrijev, J. S. Han, A. Aminbeidokhti, D. Haasmann, Quantified density of active near interface oxide traps in 4H-SiC MOS capacitors, in Mater. Sci. Forum, 858 (2016) 603–606.

[6] S. DasGupta, R. Brock, R. Kaplar, M. Marinella, M. Smith, S. Atcitty, Extraction of trapped charge in 4 H-SiC metal oxide semiconductor field effect transistors from subthreshold characteristics, Appl. Phys. Letters, 99 (2011) 023503-1–023503-3.

[7] M. J. Tadjer, K. D. Hobart, E. A. Imhoff, F. J. Kub, Temperature and time dependent threshold voltage instability in 4H-SiC power DMOSFET devices, Mater. Sci. Forum, 600 (2009) 1147–1150.

[8] A. J. Lelis, D. B. Habersat, R. Green, N. Goldsman, Temperature-dependence of SiC MOSFET threshold-voltage instability, Mater. Sci. Forum, 600 (2009) 807–810.

[9] A. J. Lelis, R. Green, D. B. Habersat, M. El, Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs, IEEE Trans. Electron Devices, 62 (2015) 316–323.