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SiC Power MOSFETs: The Current Status and the Potential for Future Development

S. Dimitrijev

Abstract - This paper reviews the advantages and the current status of commercially available SiC power MOSFETs, followed by an analysis of future trends and the potential for future development. Specifically, the review shows the advantages of the recently commercialized trench MOSFET structure and the potential for integration with SiC Schottky diodes to create fast MOSFETs. The current issues and the potential for future improvements in terms of low channel-carrier mobility and threshold-voltage drifts are also discussed.

I. INTRODUCTION

Generation, transmission, and use of electric power require different forms of power conversion, such as AC to DC (for example, conversion of main-grid power to run consumer electronics), DC-to-DC conversion from one voltage level to another, and DC to AC (for example, conversion of solar-cell power to AC grid-power). The commonly used electronic circuits for power conversion utilize switching techniques. The following are the key requirements of the controlled switch for these switching applications [1]:

1. High blocking voltage when the switch is in *off* mode.
2. Low power dissipation to enable high power-conversion efficiency.
3. High switching frequency to reduce the size and the cost of inductors and transformers.
4. Normally-off switch (the switch is in *off* mode when no controlled voltage is applied and is turned *on* by a positive controlled voltage).

These requirements are the best achieved by the MOSFET and, consequently, switching applications have been dominated by Si-based MOSFETs as the controlled switch. However, recent commercialization of SiC-based power MOSFETs offers further improvements in the performance of switching power circuits. This paper reviews the advantages of the SiC-based MOSFETs, the current commercial status of these devices, and the potential for their future development.

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II. SIC ADVANTAGE

The key advantage of SiC as a semiconductor material results from the fact that the bonds between the atoms are much stronger. This advantage is frequently quantified as a wider energy gap: 3.2 to 3.4 eV in SiC in comparison to 1.12 eV in the case of Si. However, the related critical electric field provides much more direct measure for design and comparison of power devices. The critical electric field of Si is around 30 V/μm, whereas it is around 300 V/μm in the case of SiC. This enables design of MOSFETs with smaller *on* resistances and smaller parasitic capacitances for the same blocking voltage. For example, Infineon's CoolMOS is the Si-based MOSFET with the highest blocking voltage of around V_B = 900 V. This device has *on* resistance of R_{ON} = 340 mΩ and effective output capacitance of C_{eff} =71 pF. For a comparison, CREE's SiC MOSFET with V_B = 900 V has *on* resistance of R_{ON} = 65 mΩ and effective output capacitance of C_{eff} =45 pF. The impact of the reduced *on* resistance and effective capacitance on the power dissipation can be estimated in the following way. The static power dissipation for the duty cycle δ and current I is

$$P_{stat} = \delta R_{ON} I^2 \tag{1}$$

Assuming that the delivered power P for the maximum voltage V_{max} ($V_{max}<V_B$) is

$$P = V_{\max} I \tag{2}$$

we can define the relative power dissipation as follows:

$$\frac{P_{stat}}{P} = \delta \frac{R_{ON}}{V_{\max}^2} P \tag{3}$$

Given that the dynamic power dissipation is $P_{dyn}=fC_{eff}V_{max}^2$, the relative dynamic power dissipation is

$$\frac{P_{dyn}}{P} = \frac{1}{P} fC_{eff} V_{\max}^2 \tag{4}$$

Then, the total relative power dissipation by the MOSFET is

$$\frac{P_{stat} + P_{dyn}}{P} = \delta \frac{R_{ON}}{V_{\max}^{2}} P + \frac{1}{P} f C_{eff} V_{\max}^{2} \qquad (5)$$

Using this equation, the relative power dissipations by the Infineon's CoolMOS and CREE's SiC MOSFETs are compared in Fig. 1. It can be seen that the power dissipation of the SiC MOSFET is smaller for any power level. At lower power levels, the dynamic power dissipation dominates and the SiC MOSFET is better because of its smaller output capacitance (45 pF compared to 71 pF for the CoolMOS). At higher power levels, the static power dissipation dominates and the difference between the SiC MOSFET and the Si CoolMOS is even bigger, because the *on* resistance of the SiC MOSFET is much smaller (65 mΩ compared to 340 mΩ for the CoolMOS).

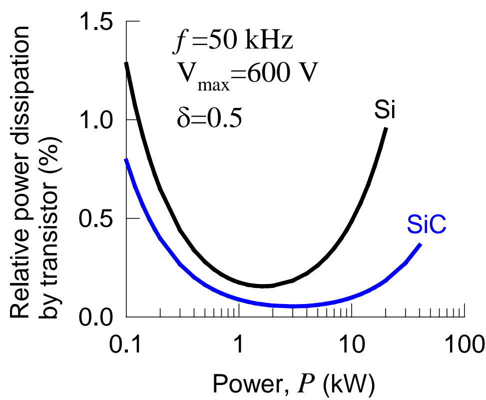

Fig. 1. Comparison between power dissipations of Si and SiC MOSFETs.

Some applications require blocking voltages in excess of 1000 V. Si-based MOSFETs cannot deliver these blocking voltages. Regarding SiC MOSFETs, they are commercially available up to 1700 V blocking voltage and 3300 V devices are being developed.

III. SiC VD-MOSFET

The standard structure of an SiC-based MOSFET replicates the VD-MOSFET structure that was developed for silicon and is shown in Fig. 2.

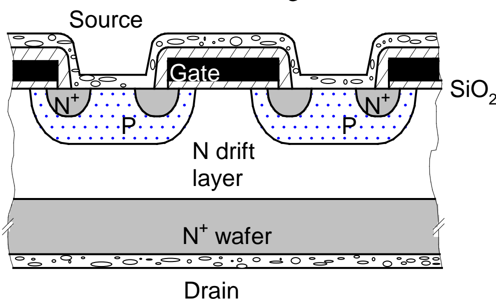

Fig. 2. VD-MOSFET as the standard power-device structure.

Commercialization of this specific structure was driven by the idea of making the smallest possible change in comparison to the successful Si-based MOSFETs—everything remains the same, apart from the semiconductor material. However, the processing situation is very much different. This structure is quite suitable for silicon, because the difference in lateral diffusions between the P-type and N^+-type regions is utilized to create the narrow P-type channel region under the gate. In the case of SiC, doping cannot be performed by diffusion, which makes it very difficult to fabricate this structure. To achieve the P-type well, multiple implantations of Al with different energies have to be performed so that the "box" profile of the P-type well can be created. More importantly, the activation of the implanted Al atoms is not simple. It requires annealing temperatures as high as 1600ºC and even then, most of the Al atoms remain inactive. The implant damage is not fully annealed and, in addition to that, if the SiC surface is not properly protected during this high-temperature annealing, unwanted sublimation of Si atoms may occur. In addition to the Al implants for the P-type well, nitrogen implantation with several energies is also needed to form the N^+ source regions. Finally, submicrometer photolithography is necessary to align the N^+ source to the edge of the P-type well and to define the channel length of the device.

In spite of the very difficult fabrication process of this device structure, this is the standard commercial SiC MOSFET today. It was initially commercialized by CREE, now Wolfspeed. Table 1 summarizes the characteristics of their latest devices. The output characteristics of the 1700-V MOSFETs are shown in Fig. 3.

TABLE I
PARAMETERS OF COMMERCIAL SIC VD-MOSFETS BY WOLFSPEED

Device Label	**CPM2-1200-0025B**
Blocking voltage	1200 V
On resistance	25 mΩ
Input capacitance	2788 pF
Output capacitance	220 pF
Chip size	4.04x6.44 mm^2
Device Label	**CPM2-1700-0045B**
Blocking voltage	1700 V
On resistance	45 mΩ
Input capacitance	3672 pF
Output capacitance	171 pF
Chip size	4.08x7.35 mm^2

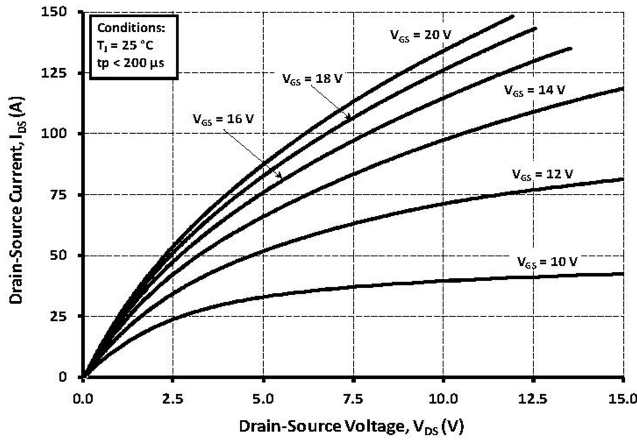

Fig. 3. The output characteristics of 1700-V SiC MOSFET by Wolfspeed (part number CPM2-1700-0045B).

IV. SIC TRENCH MOSFETS (U-MOSFETS)

An alternative structure for fabrication of SiC MOSFETs is known as trench MOSFET, or U-MOSFET. This structure is illustrated in Fig. 4.

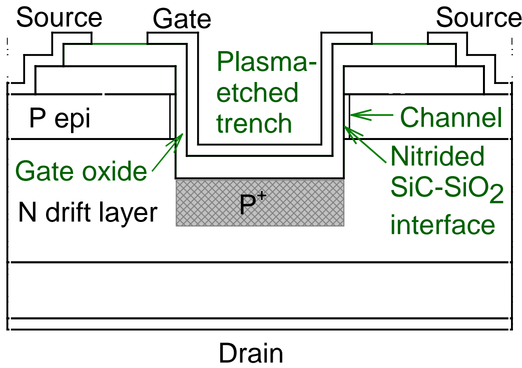

Fig. 4. Trench MOSFET (U-MOSFET): the alternative power-device structure.

The key feature in this structure is the plasma-etched trench, which enables to form the MOSFET channel on the vertical sides of the trench. Because plasma etched surfaces can be damaged and nonuniform, this structure was considered as unsuitable for commercial MOSFETs. In addition to that, a serious problem is created at the corners of the trench where the crowding of the electric field could cause gate oxide damage at high blocking voltages. In fact, there is an issue with the potential of gate-oxide breakdown at the bottom of the trench even without the field crowding at the corners. To illustrate this problem, let us observe that the drift layer of the MOSFET would be designed to support electric field that is not much smaller than the critical field of SiC. Let us assume that the design is for 70% of the critical field, which means that the electric field at the surface of the N drift layer would be E_{SiC}=210 V/µm. If this was the electric field at the bottom of the trench, the field in the gate oxide would be $E_{OX}=(\varepsilon_{SiC}/\varepsilon_{OX})E_{SiC}$=0.54 V/nm, which is unacceptably high oxide field. That is why it is necessary to protect the bottom of the trench by the P^+ region shown in Fig. 4. There are other techniques that can be used to avoid the problem of too high gate oxide field at the bottom of the trench, but this is the standard technique. The P^+ region at the bottom of the trench can be created by ion implantation into the trench after the trench is formed by plasma etching.

The other perceived problem, related to the gate oxide on the side of the trench is actually not a real problem. In fact, it turns out that the channel-carrier mobility on the vertical side is about twice as high as the channel-carrier mobility on the implanted surface in the case of the VD-MOSFET structure.

The trench structure has some obvious advantages. The on resistance in this structure is dominated by the resistance of the channel, the resistance of the drift region, and the wafer resistance. There is no resistance of the so-called JFET region between the P-wells in the case of the VD-MOSFET structure. In addition to that, the cell pitch —the distance between two source lines—is smaller than in the case of the VD-MOSFET structure. This enables larger effective channel width to be packed in the same chip area. As a result, the on resistance can be reduced by about 50% for the same chip area, as illustrated in Fig. 5.

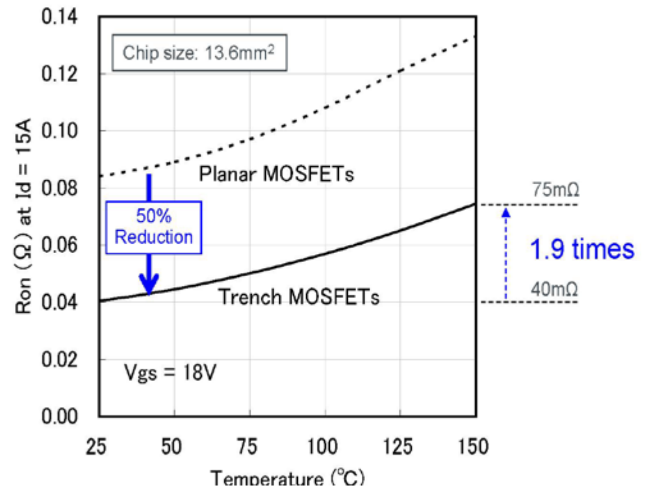

Fig. 5. Comparison of on resistances between trench MOSFET and VD-MOSFET by Rohm Co. Ltd.

The results in Fig. 5 are provided by Rohm Co. Ltd., the first company to commercialize trench SiC MOSFETs. Recently, Infineon also announced commercialization of SiC MOSFET, which is also based on the trench structure [2].

V. FAST SIC MOSFETS

The N–P junction between the N-type drain and the P-type body of a power MOSFET forms a diode, which is

used in some applications to conduct in the direction opposite to the current flow of a turned-on MOSFET. This diode is called flyback diode or free-wheeling diode. All MOSFETs have this diode, as illustrated in Fig. 6a. However, a problem with this diode could be its slow turn off due to accumulated stored charge of minority carriers. A typical solution to this problem is to connect an SiC-based Schottky-barrier diode (SBD) in parallel with the drain-to-body N–P junction diode. Because the turn-on voltage of the SBD is smaller, the internal N–P junction diode does not turn on, which avoids the formation of the stored charge. The SBD can be connected outside, but that increases the parasitic inductances, so some manufacturers package an SBD chip together with the MOSFET chip, as illustrated in Fig. 6b by Rohm Co. Ltd.

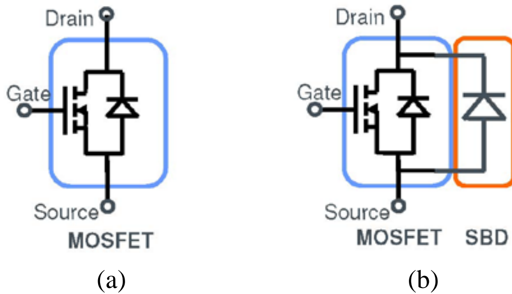

Fig. 6. MOSFET with the drain-to-body free-wheeling diode (a) and a fast MOSFET with a Schottky-barrier diode connected between the drain and the source (b).

Although not commercially available, it was demonstrated by several groups that an SBD can be integrated with the MOSFET on the same chip, which is a superior approach in terms of reduced parasitic inductances and it has potential cost benefits given that the SBD and the MOSFET can share the same edge termination. A simple integration approach, proposed by Sung and Baliga is illustrated in Fig. 7.

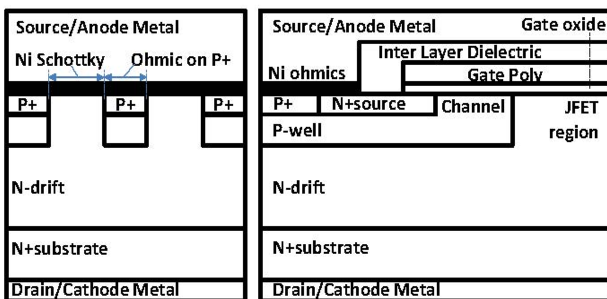

Fig. 7. Integration of a Schottky-barrier diode (the left-hand diagram) and a power VD-MOSFET (the right-hand diagram) to create a fast SiC MOSFET [3].

VI. Performance Issues

Although SiC MOSFETs provide higher blocking voltages and smaller *on* resistances in comparison the Si-based limit, the performance of the SiC MOSFETs is still below the theoretical limit of SiC. A key problem is the slow turn-on of the MOSFETs, resulting in smaller than expected drain currents. This problem is due to trapping of electrons attracted to the channel by the gate voltage, as illustrated in Fig. 8.

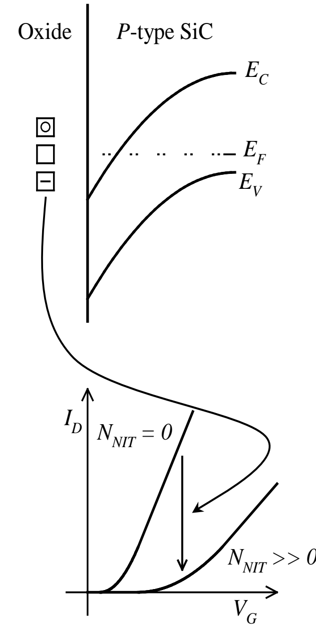

Fig. 8 Illustration of the drain-current reduction due to electron trapping by near-interface traps (NITs) with energy levels above the bottom of the conduction band [4].

The electron trapping by the near-interface traps is usually interpreted as a channel-carrier mobility reduction. Figure 9 illustrates this interpretation. As shown in Fig. 9, the density of electrons attracted to the channel by the gate voltage is equal to $N_{INV\text{-}TOT}=C_{ox}(V_G-V_{T0})/q$, where C_{ox} is the gate-oxide capacitance per unit area and V_{T0} is the ideal threshold voltage. However, for gate voltages smaller than around 5 V, all these attracted electrons are trapped by near-interface traps with energy levels below the bottom of the conduction band. The effect of this trapping is the increase in the threshold voltage from V_{T0} to V_T. If the density of NITs with the energy levels above the bottom of the conduction band were zero, the density of free electrons in the channel would be proportional to $C_{ox}(V_G-V_T)/q$, and the current increase would be according to the carrier mobility of around 150 cm^2/Vs. However, there are NITs with energy levels above the bottom of the conduction band, which continue to trap some of the attracted electrons to the channel, which reduces the expected drain current. If the channel-carrier mobility is calculated from the measured current, with the assumption that all attracted electrons are mobile, the average mobility value of around

20 cm^2/Vs is obtained. This basically means that only about (20/150)x100=13.3% of the attracted electrons to the channel are actually mobile. This shows that a significant improvement in the performance of SiC MOSFETs can be achieved if the density of near-interface traps could be reduced by an improved gate-oxidation process. However, this has proved an elusive task so far, given that the last significant improvement in this interface was achieved about twenty years ago by the introduction of the interface nitridation in NO by Dimitrijev's group [5,6].

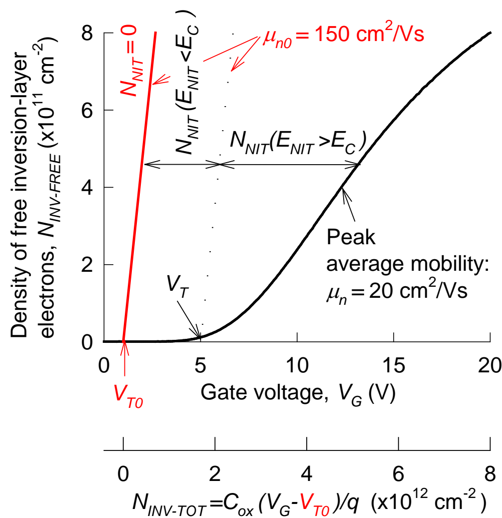

Fig. 9. Illustration of the reduction of average channel-carrier mobility due to electron trapping by near-interface traps with energy levels above the bottom of the conduction band.

VII. Reliability Issues

Gate oxides grown on SiC turned out to be quite resilient in terms of oxide breakdown. The results shown in Fig. 10 are typical and they indicate similar level of reliability to the gate oxides grown on Si substrates.

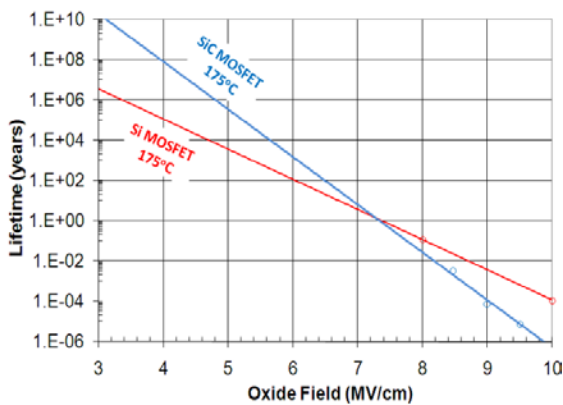

Fig. 10 Gate oxide lifetime extrapolated from high-field time-dependent dielectric breakdown (TDDB) measurements predicting sufficiently long lifetime for CREE SiC MOSFET at 175°C [7]

Another popular way of presenting oxide reliability is charge-to-breakdown characteristics. Figure 11 shows charge-to-breakdown characteristics for Rohm's commercial SiC MOSFETs.

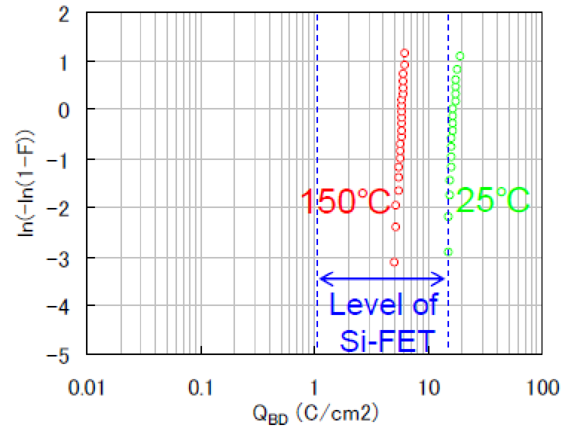

Fig. 11 Charge-to-breakdown (Q_{BD}) for Rohm's SiC MOSFETs is similar to that of Si-based MOSFETs [8]

However, a reliability problem with the gate oxides in SiC MOSFETs relates to the threshold-voltage drift [9]. The threshold-voltage drifts are observed with both negative- and positive-gate biasing at high temperatures.

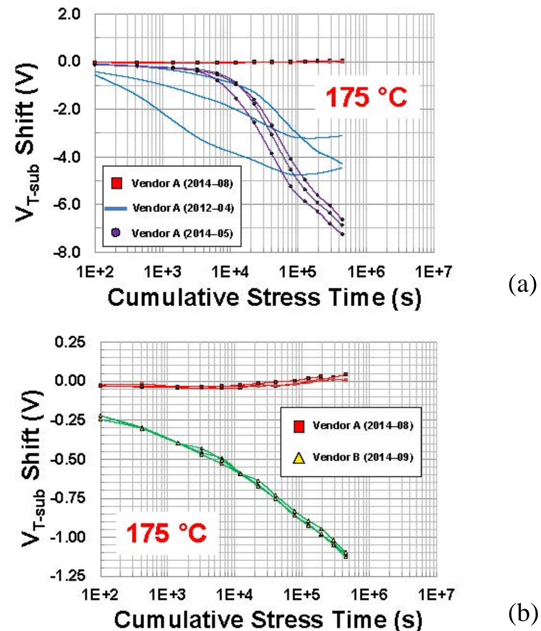

Fig. 12 Threshold-voltage shifts caused by negative-gate bias stressing at $V_G = -15$ V and 175°C for several generations of SiC MOSFETs by Vendor A (a) and a comparison of SiC MOSFETs by Vendors A and B (b) [10].

The results in Fig. 12 show that the negative-gate bias of -15 V at 175°C can lead to very significant threshold - voltage shifts in the negative direction. This is not desirable

because this kind of threshold-voltage shift can change the MOSFET from the normally-off device to normally-on device. The results shown in Fig. 12, however, also demonstrate that significant improvements in the threshold-voltage stability have been achieved.

Positive gate bias at high temperature also leads to threshold-voltage shifts, but the threshold voltages are increased in this case, as shown in Fig. 13.

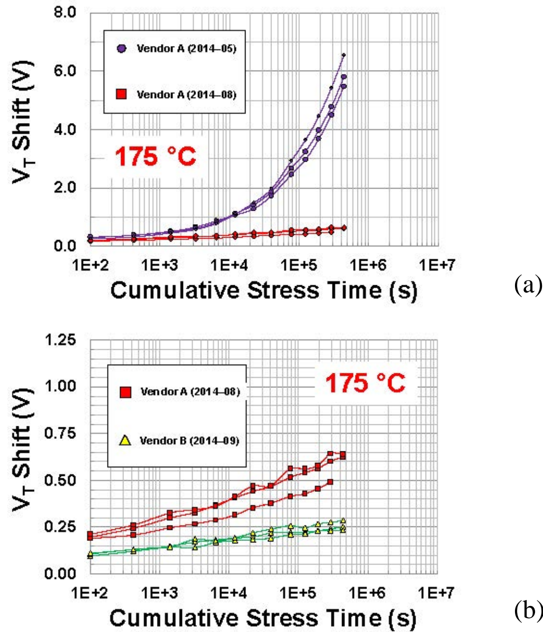

Fig. 13 Threshold-voltage shifts caused by positive-gate bias stressing at V_G = +25 V and 175°C for several generations of SiC MOSFETs by Vendor A (a) and a comparison of SiC MOSFETs by Vendors A and B (b) [10].

The threshold-voltage shifts during both negative- and positive-bias stresses can be related to the near interface traps. In the case of negative gate bias, the electric field causes electron de-trapping from the NITs, which increases the effective positive charge at the interface and reduces the threshold voltage. In the case of positive gate bias, electrons are attracted by the electric field and trapped by NITs to increase the threshold voltage. This shows that the key to further improvements in the stability of gate oxides in SiC MOSFETs is in the attempts to improve the quality of the near-interface region.

III. Conclusion

This paper has reviewed the status of commercially available SiC MOSFETs, showing that these devices exceed the theoretical limit of Si-based MOSFETs, enabling applications with higher blocking voltages and better power-conversion efficiency. The paper has described the standard VD-MOSFET structure and then argued that much better performances can be achieved in the future by adopting the trench MOSFET structure. The possibility for integration with SiC-based Schottky diode to create fast SiC MOSFETs was also discussed. Finally, the near-interface region of the gate oxide was identified as the most important area for possible future improvements in terms of both improved channel-carrier mobility (device performance) and improved threshold-voltage stability (device reliability

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