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Derivation of a Nonlinear Variance Equation and Its Application to SOI Technology

David Rowlands and Sima Dimitrijević

Abstract—An analytic nonlinear equation for variance was derived along with a method based on response surface mapping techniques to calculate the variance using the proposed equation. The technique was applied to the threshold voltage of a 0.1- μm silicon-on-insulator MOS device, and the variance value obtained was verified using Monte Carlo simulation. The threshold voltage dependence upon active-layer thickness was found to be highly nonlinear due to the device's going from the fully depleted to the partially depleted regime. Analysis of the variance showed that the effect of the nonlinear terms (18.7%) is more important than the effect of the mixed term (−0.7%) and almost as important as the contribution of the second most dominant input-process parameter (23.6%). This illustrates the importance of the proposed nonlinear equation.

Index Terms—Process fluctuations, silicon on insulator (SOI), variance.

I. INTRODUCTION

MUCH effort has been applied to scaling devices down into the deep submicrometer region to create circuits with increased density, functionality, and speed. As device dimensions decrease, the effects of fluctuations in the process parameters during manufacture will have a greater effect on the electrical characteristics of the device. The variance of an electrical parameter is an extremely important measure of the fluctuation effects [1], [2]. It can be used to monitor the process during manufacturing so that appropriate corrections can be made during later processing steps. It is also an important parameter in the design of appropriate control limits for the manufacturing process. An analytical variance model enables analysis of the variance components; hence it can be used both for inline process control and in the design of appropriate control limits.

A linear analytical model for the variance has previously been applied in the study of process fluctuations [2], [3]. However, not all processes being monitored are going to be linear. Therefore, there is a need for the development of a nonlinear variance analytic model, which will also contain information about the noncovariant mixing terms.

In this paper, an analytic third-order variance model will be derived, along with a method of obtaining numerical values for the coefficients required by the model. The third-order variance model will be illustrated through application to the threshold voltage of a 0.1- μm silicon-on-insulator (SOI) MOSFET. A Monte Carlo simulation technique will be used to determine the “experimental” variance and thereby to verify the analytic expression. The components of the analytic variance will be examined to gain further insight into the relative effects of the input parameters on this device.

II. THIRD-ORDER VARIANCE EQUATION

The variance is the second moment about the mean and can be described using the expectation [3], [4]

$$\sigma^2(x) = \varepsilon[(x - \mu)^2] = \varepsilon[x^2] - \{\varepsilon[x]\}^2. \quad (1)$$

For any function $g(x)$, the variance can be found by using a Taylor series for $g(x)$ and determining the expectation of $g(x)$ and $g^2(x)$. This will produce a single covariant term no matter what order of Taylor series is used. However, if the input variables are independent, then the covariant term will go to zero. For a function of two variables, a bivariate Taylor series needs to be used. It should be noted that higher order Taylor series will produce noncovariant terms consisting of a mixture of both input variables. The order of the variance equation is determined by the order of the Taylor series used in its derivation. Using third-order Taylor series, the following equation is obtained:

$$\begin{aligned} \sigma_g^2 = & \sigma_x^2 \left(\frac{\partial g(x, y)}{\partial x} \right)^2 + \sigma_y^2 \left(\frac{\partial g(x, y)}{\partial y} \right)^2 && \text{first order} \\ & + (\sigma_x^2)^2 \left[\frac{1}{2} \left(\frac{\partial^2 g(x, y)}{\partial x^2} \right)^2 + \frac{\partial g(x, y)}{\partial x} \frac{\partial^3 g(x, y)}{\partial x^3} \right] \\ & + (\sigma_y^2)^2 \left[\frac{1}{2} \left(\frac{\partial^2 g(x, y)}{\partial y^2} \right)^2 + \frac{\partial g(x, y)}{\partial y} \frac{\partial^3 g(x, y)}{\partial y^3} \right] && \text{second order} \\ & + (\sigma_x^2)^3 \left[\frac{1}{3} \left(\frac{\partial^3 g(x, y)}{\partial x^3} \right)^2 \right] \\ & + (\sigma_y^2)^3 \left[\frac{1}{3} \left(\frac{\partial^3 g(x, y)}{\partial y^3} \right)^2 \right] && \text{third order} \\ & + \sigma_x^2 \sigma_y^2 \left[\left(\frac{\partial^2 g(x, y)}{\partial x \partial y} \right)^2 + \frac{\partial g(x, y)}{\partial x} \frac{\partial^3 g(x, y)}{\partial x \partial y^2} \right. \\ & \quad \left. + \frac{\partial g(x, y)}{\partial y} \frac{\partial^3 g(x, y)}{\partial x^2 \partial y} \right] \\ & + (\sigma_x^2)^2 \sigma_y^2 \left[\frac{3}{4} \left(\frac{\partial^3 g(x, y)}{\partial x^2 \partial y} \right)^2 \right. \\ & \quad \left. + \frac{1}{2} \left(\frac{\partial^3 g(x, y)}{\partial x^3} \frac{\partial^3 g(x, y)}{\partial x \partial y^2} \right) \right] && \text{Mixed} \\ & + \sigma_x^2 (\sigma_y^2)^2 \left[\frac{3}{4} \left(\frac{\partial^3 g(x, y)}{\partial x \partial y^2} \right)^2 \right. \\ & \quad \left. + \frac{1}{2} \left(\frac{\partial^3 g(x, y)}{\partial y^3} \frac{\partial^3 g(x, y)}{\partial x^2 \partial y} \right) \right]. \quad (2) \end{aligned}$$

Applying (2) to process control, x and y refer to input processing parameters such as temperature, time, dose, energy, etc., g refers to an electrical parameter such as threshold voltage, and the values of the differentials (variance equation coefficients) need to be determined to represent the specific case being modeled (technology, device, nominal process parameter, etc.). To determine values for the differentials, we propose a method based upon an adapted *response surface mapping* (RSM) technique. RSM techniques require a surface to be created and

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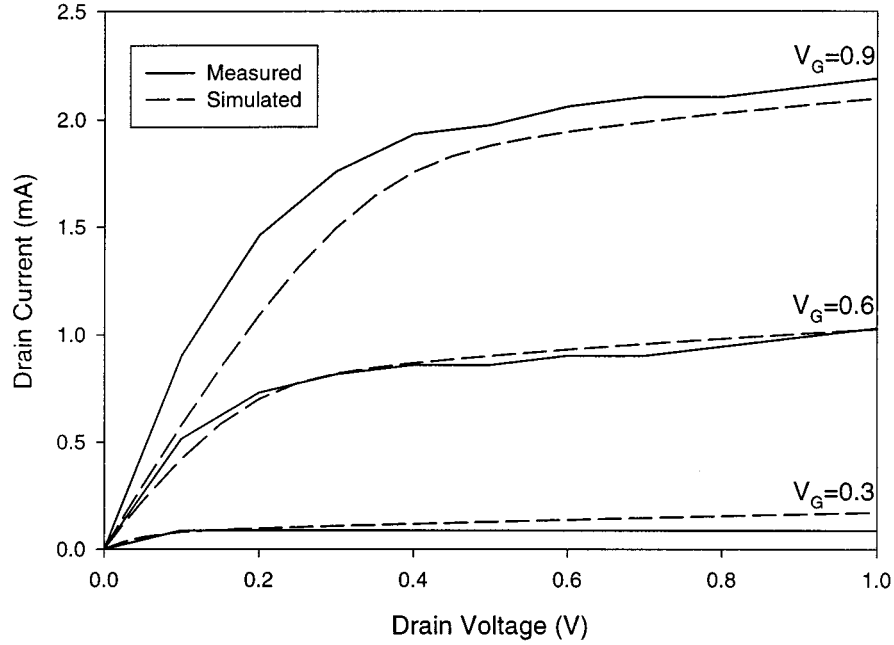
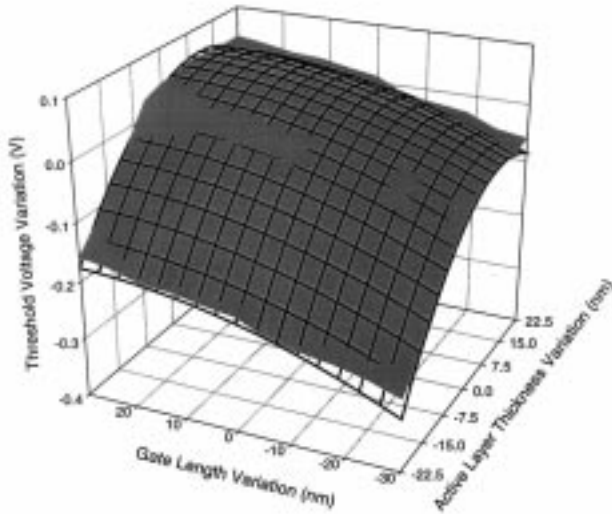


Fig. 1. Output characteristics of the measured and simulated devices.


 Fig. 2. Threshold voltage dependence upon active-layer thickness and gate length using $T_{\text{nom}} = 70$ nm and $L_{\text{nom}} = 100$ nm; the simulation data are shown by the shaded surface, while the polynomial fit is shown by the lines.

a suitable polynomial mapped to that surface [11]–[13]. Through the proper application of *design of experiment techniques*, the number of points used to create the surface can be minimized. For a nonlinear surface, the following polynomial can be used to fit to the response surface:

$$z(x, y) = xA + yB + \frac{1}{2}x^2C + \frac{1}{2}y^2D + \frac{1}{6}x^3E + \frac{1}{6}y^3F + xyG + \frac{1}{2}x^2yH + \frac{1}{2}xy^2I. \quad (3)$$

 TABLE I
 FLUCTUATION VALUES OF PROCESS
 PARAMETERS [1], [2]

Input Parameter	Standard Deviation
Time	1s
Temperature	0.5°C
Energy	1%
Dose	1%
Poly Gate Length	10nm
Active Layer Thickness	7.5nm

This polynomial is based on a Taylor series in two variables

$$\begin{aligned} z(x, y) &= x \frac{\partial z(x, y)}{\partial x} + y \frac{\partial z(x, y)}{\partial y} + \frac{1}{2}x^2 \frac{\partial^2 z(x, y)}{\partial x^2} \\ &+ \frac{1}{2}y^2 \frac{\partial^2 z(x, y)}{\partial y^2} + \frac{1}{6}x^3 \frac{\partial^3 z(x, y)}{\partial x^3} + \frac{1}{6}y^3 \frac{\partial^3 z(x, y)}{\partial y^3} \\ &+ xy \frac{\partial^2 z(x, y)}{\partial x \partial y} + \frac{1}{2}x^2y \frac{\partial^3 z(x, y)}{\partial x^2 \partial y} + \frac{1}{2}xy^2 \frac{\partial^3 z(x, y)}{\partial x \partial y^2}. \end{aligned} \quad (4)$$

Comparing (3) to (4), we find that the fitting coefficients correspond directly to the differentials (variance equation coefficients). Therefore,

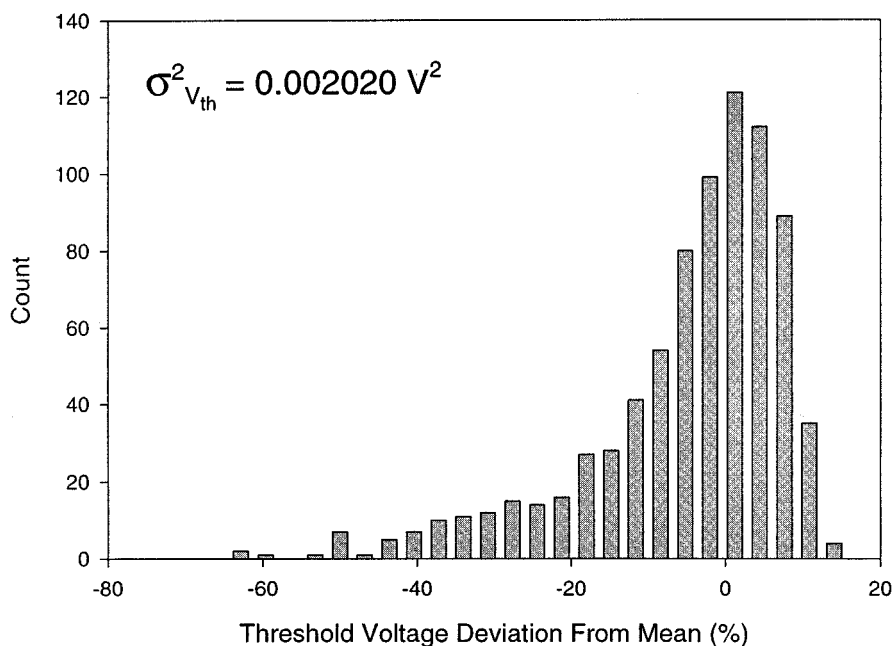


Fig. 3. Histogram for the threshold voltage with all input parameters randomized.

values for the differentials (variance equation coefficients) in (2) can be obtained by fitting the polynomial given by (3).

III. APPLICATION

To illustrate an application of the derived equation, we will calculate an electrical parameter's variance based upon the known variance of two independent input processing parameters. The threshold voltage is an extremely important parameter in the operation of any MOSFET, and a great deal of effort is employed to remove the sensitivity of the threshold voltage to input process fluctuations. Therefore, it was decided to illustrate and verify the nonlinear variance equation using the threshold voltage. The device chosen for examination was the $0.1\text{-}\mu\text{m}$ SOI NMOS device developed by IBM [7]–[10] due to the sensitivity of the threshold voltage to the SOI process. The thicknesses of the active top silicon layer (T_{Si}) and the gate length (L_g) were selected as the two independent input processing parameters because they were found as the dominant sources of threshold voltage fluctuations.

The $0.1\text{-}\mu\text{m}$ SOI NMOS device was simulated using TSUPREM4 (a process simulator) and MEDICI (a device simulator). For the simulation to be meaningful, the processing steps and mobility models had to be tuned until the simulated electrical characteristics matched the known measured characteristics for the device [7]. In this case, the standard mobility models were used with no adjustment of their associated mobility parameters. However, a value for the interface traps of $1 \times 10^{10} \text{ cm}^{-2}$ was used to give more a realistic simulation. The simulated and measured output characteristics can be seen in Fig. 1. The characteristics are fairly well matched in the saturation region, which is the area of interest in this paper. The match in the linear region could be improved by adjusting the mobility parameters; however, it was not deemed necessary due to the device's operating in the saturated region.

Simulations were used to generate a surface corresponding to the threshold voltage as a function of active-layer thickness and gate length. To generate the surface, the input parameters were stepped through their entire possible range of values. Since these input parameters assume a normal distribution, then stepping through $\pm 3\sigma$ will account for 99.97% of the possible values. The standard deviations of the input parameters were set to $\sigma_T = 7.5 \text{ nm}$ and $\sigma_L = 10 \text{ nm}$

[1], [2]. The obtained surface is shown in Fig. 2. It can be seen that the dependence upon the gate length is slightly nonlinear, whereas the dependence upon the active layer thickness is highly nonlinear.

The nonlinear (third-order) variance can be obtained by fitting a third-order polynomial to the surface to determine the differentials. The form of the third-order polynomial is given in (3). The polynomial was fit to the surface giving $A = 4.566 \times 10^{-4} \text{ V/m}$, $B = 2.106 \times 10^{-4} \text{ V/m}$, $C = -4.290 \times 10^{-6} \text{ Vm}^{-2}$, $D = -6.148 \times 10^{-7} \text{ Vm}^{-2}$, $E = -7.648 \times 10^{-8} \text{ Vm}^{-3}$, $F = 3.880 \times 10^{-9} \text{ Vm}^{-3}$, $G = -7.150 \times 10^{-10} \text{ Vm}^{-2}$, $H = -2.008 \times 10^{-10} \text{ Vm}^{-3}$, and $I = 1.753 \times 10^{-10} \text{ Vm}^{-3}$ with a regression coefficient $r^2 = 0.974$. The fit to the surface is also shown in Fig. 2. Substituting these values for the differentials and the values of σ_T and σ_L into (2) gives a variance of $\sigma_{V_{th}}^2 = 0.001974 \text{ V}^2$.

IV. VERIFICATION

Monte Carlo techniques were used to obtain an "experimental" threshold voltage distribution, as determined by random changes in the input process parameters. A single Monte Carlo cycle consisted of the random generation of a set of input process parameters, followed by simulation to obtain a threshold voltage value. For the Monte Carlo technique to be meaningful, a large number of cycles had to be performed to create a threshold voltage distribution. Normal distributions were assumed for the input process parameters, with the values for the standard deviations given in Table I. [1], [2]. The threshold voltage distribution obtained after 800 Monte Carlo cycles is shown in Fig. 3. It can be seen that the histogram is skewed to the left. This is due to the shape of the response surface, whose gradient is larger for the negative values of standard deviation than for the positive values.

When applying the analytical nonlinear variance equation, it was assumed that the active-layer thickness and channel length would be the dominant process parameters. To verify this assumption, the threshold voltage variance was determined with all the input process parameters randomized and was compared to the variance with *only* the active-layer thickness and gate length randomized. The difference corresponding to the effect of all the other input parameters apart from the active-layer thickness and the gate length. It was found that the ac-

TABLE II
CONTRIBUTION OF DIFFERENT COMPONENTS OF NONLINEAR VARIANCE EQUATION

Component of Analytic equation	Value (V^2)	% of total variance
3 rd order complete equation	1.9736×10^{-3}	-
2 nd order	1.9727×10^{-3}	99.96
1st order	1.6162×10^{-3}	81.89
mixed terms	-1.3319×10^{-5}	-0.68
3 rd order - silicon thickness only	1.5208×10^{-3}	77.06
3 rd order - gate length only	4.6612×10^{-4}	23.62

tive-layer thickness and gate length contributed 81.2% to the threshold voltage variance, while the other input process parameters contributed 18.8% to the threshold voltage variance.

To verify the accuracy of the analytic variance equation, it was compared to the Monte Carlo result (Fig. 3). The difference between the third-order analytic and the Monte Carlo values of variance is only 2%, indicating the accuracy of the nonlinear equation.

V. ANALYSIS BASED ON THE ANALYTIC NONLINEAR VARIANCE EQUATION

The contributions of different components of the analytic nonlinear variance equation, as shown in Table II, can provide some very useful information. To begin with, it can be seen that the difference between the second-order and third-order equations is insignificant, indicating very fast convergence, and proving that the neglected higher order terms in the Taylor series do not add up to a significant error. Nonetheless, the linear terms can account only for about 82% of the total variance, meaning that the application of the linear equation in this case would lead to significant errors.

The contribution of the mixing terms is also a very interesting result. Given that the gate length influences the threshold voltage through the effect of "charge sharing," which can be significantly influenced by the active silicon thickness, there may be an expectation that the mixing terms will take a significant role in the total variance. Table II shows that the mixed terms have *negative contribution*, meaning the opposing influences of the gate length and silicon thickness reduce the variance. However, the absolute value of this contribution, being 0.86%, is insignificant compared to the other factors.

The proposed analytical variance equation can also be used to extract relative contributions of individual process parameters. Table II shows the contributions from the silicon thickness alone, as well as from the gate length alone. It can be seen that the silicon thickness accounts for about 77% of the total threshold voltage variance. This means that this is the parameter to address if a reduction in the threshold voltage variance is needed. Referring to the response surface shown in Fig. 2, it is obvious that the silicon thickness should be increased to decrease the threshold voltage variance.

Finally, it is interesting to note that the nonlinear terms (18.1%) are almost as important as the contribution by the gate length (23.6%), which is the second most dominant process parameter.

VI. CONCLUSION

An analytic equation for third-order variance was derived [(2)] and its application illustrated for the threshold voltage of a 0.1- μm SOI MOSFET device. The equation was verified using Monte Carlo methods to replace experimentation. Analysis of the components of the nonlinear analytic variance equation revealed that the active-layer thickness and the gate length both act to increase the spread of the threshold voltage, whereas the mixed term acts to reduce the spread of the threshold voltage. This reduction is due to the effect of the active-layer thickness opposing the effect of the gate length. However, the analysis also showed that the contribution of the mixed terms is negligible when compared to the other factors. It was also found that the contribution of the second-order terms is almost as important as the contribution of the gate length, which is the second most dominant parameter. This shows that a higher order variance equation is required and that a good fit to the surface is essential.

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REFERENCES

- [1] T. J. Sander and M. J. Phelps, "Simulation of the effects of manufacturing process variations on the characteristics of SOI MOSFETs," in *Proc. 1995 IEEE Int. SOI Conf.*, Oct. 1995, pp. 24–25.
- [2] R. Sitte, S. Dimitrijevic, and H. B. Harrison, "Device parameter changes caused by manufacturing fluctuations of deep submicron MOSFET's," *IEEE Trans. Electron. Devices*, vol. 41, pp. 2210–2215, Nov. 1994.
- [3] H. C. De Graaff and F. M. Klaassen, *Compact Transistor Modeling for Circuit Design*. New York: Springer-Verlag/Wien, 1990.
- [4] A. M. Mood, F. A. Graybill, and D. C. Boes, *Introduction to the Theory of Statistics*, 3rd ed. Tokyo, Japan: McGraw-Hill, 1974.
- [5] J.-P. Collinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Norwell, MA: Kluwer Academic, 1991.
- [6] C. H. Wann, K. Noda, T. Tanuka, M. Yoshida, and C. Hu, "A comparative study of advance MOSFET concepts," *IEEE Trans. Electron. Devices*, vol. 43, pp. 1742–1753, Oct. 1996.
- [7] G. Shahidi, C. Anderson, B. Chappell, T. Chappell, J. Comfort, B. Davari, R. Dennard, R. Franch, P. McFarland, J. Neely, T. Ning, M. Polcari, and J. Warnock, "A room temperature 0.1 μm CMOS on SOI," *IEEE Trans. Electron. Devices*, vol. 41, pp. 2405–2411, Dec. 1994.
- [8] G. Shahidi, J. Warnock, S. Fischer, P. McFarland, A. Acovic, S. Subbanna, E. Gannin, E. Crabbe, J. Comfort, J. Sun, T. Ning, and B. Divari, "High-performance devices for a 0.15- μm CMOS technology," *IEEE Electron. Device Lett.*, vol. 14, pp. 466–468, Oct. 1993.

- [9] G. Shahidi, B. Davari, T. Bucelot, P. Ronshiem, P. Coane, S. Pollack, C. Blair, B. Clark, and H. Hansen, "Indium channel implant for improved short-channel behavior of submicrometer NMOSFETs," *IEEE Electron. Devices Lett.*, vol. 14, pp. 409–411, Aug. 1993.
- [10] D. Antoniadis and I. Moskowitz, "Diffusion of indium in silicon inert and oxidizing ambients," *J. Appl. Phys.*, vol. 53, no. 12, pp. 9214–9216, Dec. 1982.
- [11] G. J. Gaston and A. J. Walton, "The integration of simulation and response surface methodology for the optimization of IC processes," *IEEE Trans. Semiconduct. Manufact.*, vol. 7, pp. 22–33, Feb. 1994.
- [12] A. J. Walton, M. Fallon, M. I. Newsam, R. S. Ferguson, and D. Sprevak, "Procedures for the development of manufacturable IC processes," in *Proc. 13th Australian Microelectronics Conf.*, Adelaide, 1995.
- [13] G. E. P. Box and N. R. Draper, *Empirical Model-Building and Response Surface*. New York: Wiley, 1978.
- [14] D. Burnett, K. Erington, C. Subramanian, and K. Baker, "Implications of fundamental threshold voltage variations for high-density SRAM and logic circuits," in *Symp. VLSI Technology Dig. Tech. Papers*, 1994, pp. 15–16.
- [15] H. Wong and Y. Taur, "Three-dimensional atomistic simulation of discrete random dopant distribution effects in sub-0.1 μm MOSFET's," *Int. Electron Devices Meeting Tech. Dig.*, pp. 705–708, 1993.
- [16] T. Mizuno, J. Okamura, and A. Toriumi, "Experimental study of threshold voltage fluctuation using an 8K MOSFET array," *Symp. VLSI Technology Dig. Tech. Papers*, pp. 41–42, 1993.
- [17] L. T. Su, J. B. Jacobs, J. Chung, and D. Antoniadis, "Short channel effects in deep-submicrometer SOI MOSFETs," in *Proc. 1993 IEEE Int. SOI Conf.*, pp. 112–113.