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Gate Capacitances of High Electron Mobility Transistors

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Abstract - The gate-drain capacitance and the source-drain capacitance of High Electron Mobility transistors have been measured on a computer-aided measurement system. The variation of these capacitances with transistor bias voltages is explained and compared with the trend predicted by a capacitance model used in literature. Differences in measured and calculated results arise from the assumptions used in the model. A modification to include the influence of channel potential profile is proposed.

Keywords: Gate capacitance, Gate-drain capacitance, Source-drain capacitance, HEMT capacitance.

1. INTRODUCTION

High Electron Mobility transistors (HEMTs) are used in high gigaHertz amplifier applications. At these high frequencies, the gate-drain capacitance, C_{gd}, and gate-source capacitance, C_{gs}, directly affect the frequency response of the amplifier. This is obvious from the small signal equivalent circuit of the transistor shown in Figure 1 [1]. C_{gs} shunts the input signal and C_{gd} compromises gain through negative feedback, or equivalently reduces gain through the Miller effect. A knowledge of these capacitances is then important for accurate modelling of HEMT circuits. Calculation of these capacitances is quite involved as device structures are generally not known to the user and also the device physics involved is complex. But these capacitances can be measures with comparative ease if a measurement facility is properly set up.

A simplified structure of a HEMT is shown in Figure 2 [2]. In the AlGaAs-GaAs conventional system, a heterojunction is formed at the AlGaAs-GaAs interface. Due to the difference in band-gap energies, a triangular barrier exists at the interface with high density of states for electrons. Electrons from the AlGaAs layer migrate to these states where they form a thin sheet of highly mobile carriers known as two dimensional electron gas (2-DEG). The enhanced mobility comes from the fact that these carriers are physically removed from the parent atoms and are located in a region where the semiconductor is almost pure and lattice scattering is minimal. The control of the electron gas comes through a Schottky gate contact to the AlGaAs layer to provide the normal transistor action. The gate capacitance components are shown in the figure. The gate-drain capacitance C_{gd} is the sum of C_{gd}' and the fringing capacitance C_{gdo} between the gate and the drain. The gate-source capacitance is the sum of the C_{gs}' and the fringing capacitance C_{gso} between the gate and the source.

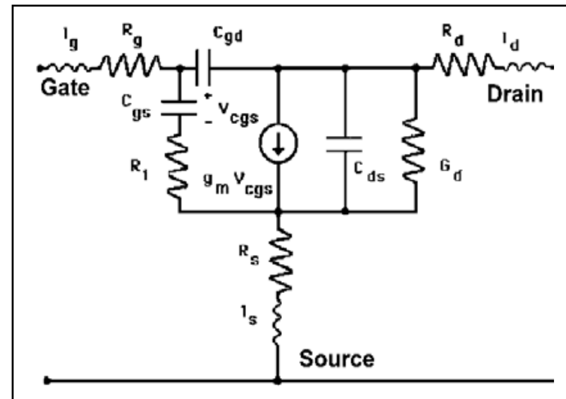

Fig. 1. AC equivalent circuit of HEMT

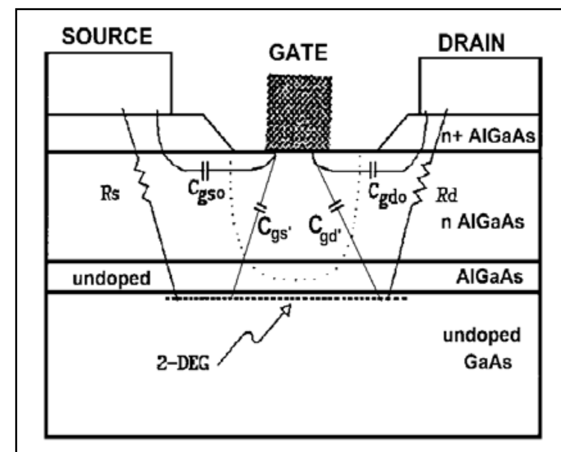

Fig. 2. Structure of HEMT

Analytical models for the gate capacitances reported in the literature are based on formulations similar to that used by Meyer for MOSFETs [4]. These are of the form as follows [5,6]:

$$C_{gs} = \frac{2}{3} C_g \{1 - \frac{(V_{dsat} - V_{ds})^2}{(2V_{dsat} - V_{ds})^2}\} + C_{gso} \quad (1)$$

for $V_{ds} < V_{dsat}$, and

$$C_{gs} = \frac{2}{3} C_g + C_{gso} \quad \text{for} \quad V_{ds} \geq V_{dsat} \quad (2)$$

$$C_{gd} = \frac{2}{3} C_g \{1 - \frac{V_{dsat}^2}{(2V_{dsat} - V_{ds})^2}\} + C_{gdo} \quad (3)$$

for $V_{ds} < V_{dsat}$, and

$$C_{gd} = C_{gdo} \quad \text{for} \quad V_{ds} \geq V_{dsat} \quad (4)$$

where C_g is the total gate capacitance, V_{ds} is the drain-source voltage, and V_{dsat} is the saturation drain voltage at a given gate voltage.

In this paper the measured values of C_{gs} and C_{gd} are presented and then compared with the analytical models (1)-(4). It is argued that the channel capacitance at different points along the channel of the device need to be taken into account for good experimental agreement. An expression for the calculation of the gate capacitance including the effect of channel potential is proposed.

2. MEASUREMENT SETUP

The measurement setup consists of a HP4284A LCR meter, A HP4145A Semiconductor Parameter Analyser, and a probing station for contacting the devices in chip form. Instruments are controlled by a computer through a HP Interface Bus. For simplicity of measurement, C_{gd} and C_{gs} are measured on the same source/drain contact, only the terminal voltages are changed to bias it as a source or as a drain. The simplified connection diagrams for the measurement are shown in Figure 3 [3].

The ac signal, the dc bias sources and the current sensor are internal to the LCR meter. The SMU is a dc voltage source of the parameter analyser. The LCR meter calculates the capacitance from the signal voltage and the resulting signal current. It has been found important that in the measurement of the very small capacitances of the HEMT devices, the LCR meter is balanced with all interconnecting wires in place. To reduce inter-probe capacitances, coaxial probes are preferred. Firm probe contacts are essential to reduce contact resistances for accurate results.

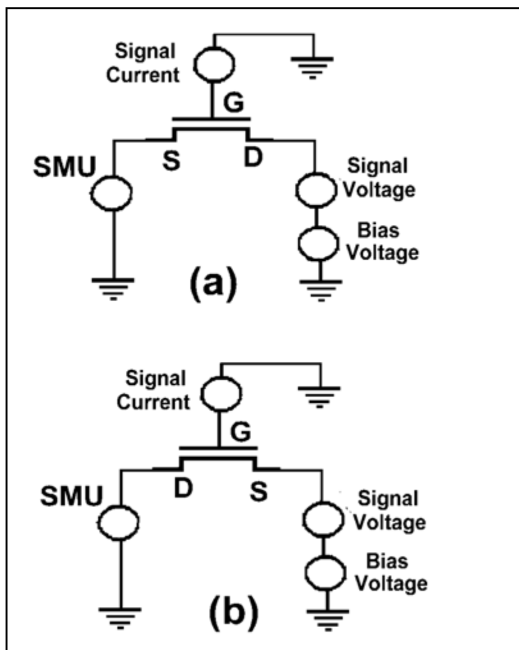

Fig. 3. Measurement setup for (a) C_{gd} and (b) C_{gs}

3. RESULTS

Gate capacitance measurements were made on Fujitsu FHX35X HEMTs in chip form. Figure 4 shows the variation of C_{gd}. with V_{ds}, with gate voltage, V_{gs}, as a parameter, while Figure 5 shows the variation of C_{gs} with V_{ds} with gate voltage as a parameter.

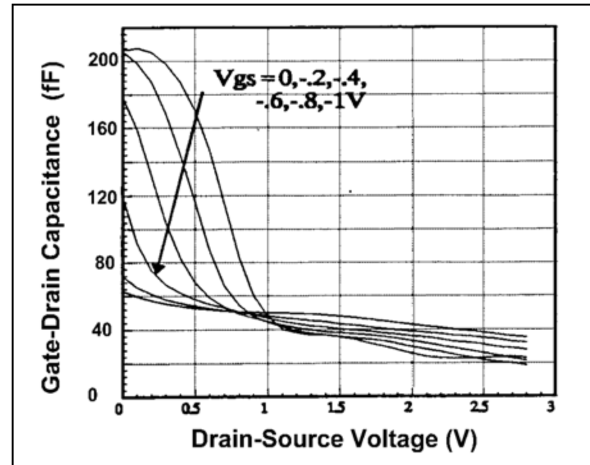

Fig. 4. Gate-Drain Capacitance

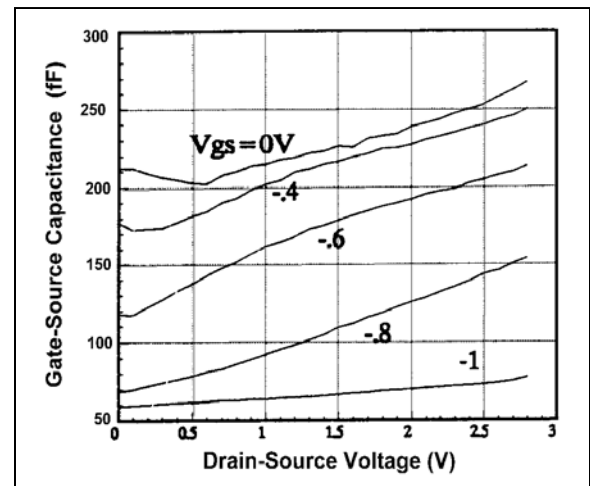

Fig. 5. Gate-Source Capacitance

Figure 4 shows that C_{gd} decreases rapidly as V_{ds} increases from zero for a given gate voltage V_{gs}. The capacitance levels off at higher value of V_{ds}. Also, as V_{gs} is reduced (more negative), C_{gd} is also reduced at zero drain voltage. For V_{gs} less than -1V for which the device is in pinch-off, C_{gd} is low and nearly independent of V_{ds}. These features are explained with reference to the ac signal potential across the channel for C_{gd} measurement, depicted in Figure 6.

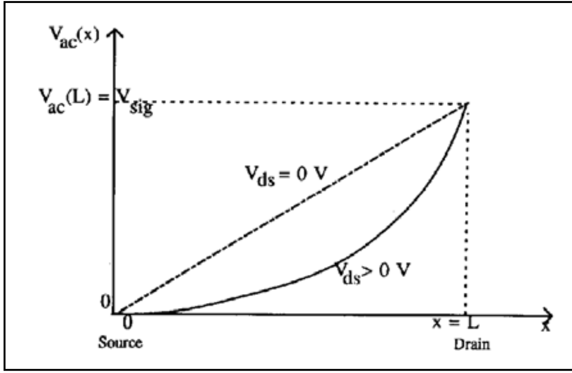

Fig. 6. AC Channel Profile.

Drain-source capacitance C_{gd} can be expressed in terms of the ac channel potential distribution $V_{ac}(x)$ of Fig. 6 when a signal V_{sig} is applied to the drain for C_{gd} measurement. In this simple model where AlGaAs control layer is totally depleted and 2-DEG is a sheet charge located at the interface, C_{gd}' can be shown to be given by:

$$C_{gd}' = \frac{C_d W}{V_{sig}} \int_0^L V_{ac}(x)dx \quad (5)$$

where C_d is the per unit area depletion capacitance of the AlGaAs layer taken to be constant for the whole length of the channel, W and L are the width and the length of the device, respectively. It is seen that the measured capacitance is proportional to the area under the curve in Fig. 6. For the bias condition $V_{ds}=V_{gs}=0$, there is a uniform channel under the gate. The $V_{ac}(x)$ changes linearly across the channel, as shown by broken lines. The measured capacitance is 1/2 C_g. As V_{ds} increases in the linear range of operation, the 2-DEG near the drain gradually depletes. This increases the channel resistance near the drain end. A larger part of the signal will drop near the drain giving the profile shown by solid line in Fig. 6. This indicates that C_{gd} will decrease, as seen in the measured results. The measured results also show that this decrease is complete by the time the drain voltage reaches the saturation value. In the saturation region, C_{gd} is low and close to C_{gdo}. Further increase of V_{ds} brings only a small decrease in C_{gd} due to a very small increase in depletion region near the drain.

The variation in C_{gs} has the general trend that it increases with increasing V_{ds} for a given V_{gs}. This can be explained as follows. Increase in V_{ds} causes the 2-DEG at the drain end of the channel to decrease and eventually to disappear. The ac signal applied to the source will be dropped mostly across the drain end of the channel, Fig. 6. The area under the ac potential profile will increase. This leads to an increase in C_{gs}. For a given V_{ds}, C_{gs} decreases with increasing negative V_{gs}, mainly because of the decrease of C_g. For small V_{gs}, such as zero volt, C_{gs} is seen to decrease slightly when V_{ds} changes from 0 to 0.5V. This decrease can be attributed to the fact that with zero V_{gs} the depletion mode HEMT channel is fully open and the increase of the drain voltage is felt at the source end. A slight change in source potential has the effect that it reduces the channel capacitance C_d slightly, reducing the source-gate capacitance with a corresponding small amount.

4. COMPARISON OF RESULTS

The modified Meyer model (1)-(4) assumes a constant C_g for a given bias condition. The equivalence of this in (5) is that C_d is constant across the channel. For comparison purposes, the intrinsic C_g is obtained from the measured values for $V_{gs}=V_{ds}=0$. The experimental value of C_{gd} at Vgs=0V and Vds=2V from Fig. 4 is taken as the value of the stray capacitance comprising of the external fringe capacitance and the small internal fringe capacitance associated with the drain. The stray capacitance is then added to the computed C_{gd} and C_{gs} using (1)-(4). These are shown in Figure 7. It is seen that although the trends of the analytical expressions are correct, there is an overestimation of C_{gs} and an underestimation of C_{gd}. Since C_{gd} is magnified by the Miller effect, an underestimation of this quantity is likely to lead to a prediction of a better frequency response of HEMT circuits than the actual response.

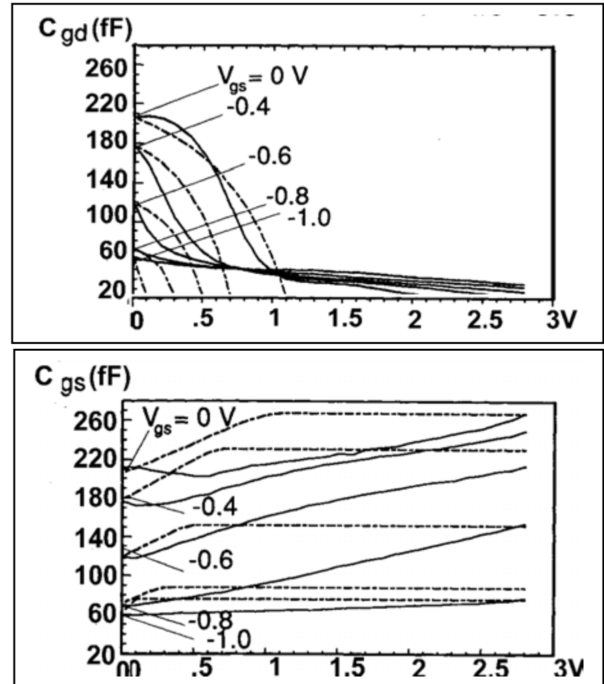

Fig. 7. Calculated and measured results top- C_{gd}, bottom- C_{gs} versus Drain-Source voltage.

The main source of discrepancy in the model is the assumption of constant C_d for the whole length of the channel. Representing the dc channel potential at point x in the channel by V(x), the effective gate drive at this point is V_{gs}-V(x) and C_d is a function of this gate drive. Equation (5) should then be modified to:

$$C_{gd}' = \frac{W}{V_{sig}} \int_o^L C_d V_{ac}(x) dx \qquad (6)$$

where $C_d(V_{gs}-V(x))$ should be obtained either from experimental data or from an analytical model. V(x) or $V_{ac}(x)$ is unfortunately not available from circuit models of field effect transistors. Methods to extract this information analytically or from measured results is a topic for further work.

5. CONCLUSIONS

The results of measurements of the gate-drain and gate-source capacitances of HEMTs have been presented. These results are compared with calculations using an analytical capacitance model used in the literature. The differences in results have been attributed to the model's assumption of constant channel capacitance for the whole length of the gate. This capacitance is dependent on the structure of the heterojunction and also on the potential distribution along the channel due to transistor's dc bias. An expression to calculate the channel capacitance including the effect of the potential distribution along the channel is given.

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