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Specific contact resistance of ohmic contacts to n-type SiC membranes

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ABSTRACT

Membranes of epitaxial SiC have been used as a means of eliminating the leakage current into the Si substrate during circular transmission line model (CTLM) measurements. In the n^{+}-3C-SiC/ Si wafers, the Si substrate was etched in a patterned window with dimensions up to 10 mm x 15 mm^2. An array of CTLM metal contacts was then deposited onto the upper surface of the n^+-SiC membrane. The CTLM contacts on the membrane have shown an ohmic current/ voltage response while electrodes located on the adjacent substrate were non-ohmic. Values of ρ_c were measured directly on the membranes. These results have shown a significant increase in the current flow below the metal contacts due to the presence of the Si substrate.

INTRODUCTION

Silicon carbide (SiC) has become an important structural material in micro-electromechanical systems (MEMs). The mechanical strength and thermal stability of SiC have enabled the fabrication of MEMs devices with significantly greater resistance to harsh environments than for silicon. SiC-based devices have shown a distinct advantage over silicon at elevated temperatures above 300 °C, in corrosive atmospheres and in components subject to mechanical sliding contact and wear. A further advantage of SiC in the fabrication of MEMs devices has been the compatibility of the micromachining processes with equivalent methods used for Si. The wide range of MEMs devices based on SiC has been reviewed by Camilla et al. [1] and Zappe [2]. Examples of SiC devices have included automotive pressure sensors used in harsh environments, electronics for high radiation applications and microswitches with improved power capability [1,2]. Other applications of SiC in biological and biomedical MEMs have been based on the chemical inertness and biocompatibility of the surfaces [1,3].

An essential requirement in the fabrication of many of these devices in SiC is the formation of ohmic contacts with low specific contact resistance (ρ_c). For n-type SiC, the metal Ni has been reported to form low resistivity ohmic contacts after annealing [4,9-10]. Other metal systems including Pd [5,11] and Ti/Ni/Ti/Au [6] have resulted in ohmic contacts at significantly lower annealing temperatures than for Ni. However, in previously reported measurements of ρ_c in n-SiC using the transmission line model (TLM), the magnitude of leakage current within the substrate has remained an uncontrolled variable. In this paper, we report for the first time on the use of a membrane of epitaxial n^+-SiC as a means of eliminating leakage current in the substrate during TLM measurements. In these membrane structures, the Si substrate was removed from a window region of the n^+-SiC/ Si wafer by backside etching. An array of circular TLM patterns as defined by Reeves [7] was then deposited directly onto the upper surface of the n^+-SiC. The electrical contact parameters have been measured on both the n^+-SiC membrane and on the adjacent non-etched regions of wafer with underlying n^+-SiC/Si.

EXPERIMENTAL DETAILS

The epitaxial layers of n-type 3C-SiC were grown on substrates of p-Si <100> in a hot wall low pressure chemical vapour deposition (LPCVD) reactor at the Queensland Microtechnology Facility, Griffith University [8]. The films of n^+-SiC were deposited to a thickness of 0.285, 0.950 or 1.18 µm on both sides of the Si substrate. Hot probe measurements have shown a doping level of ~1-2 x 10^{19} cm^{-3}. The wafers were then diced into rectangles with dimensions of 15 x 20 mm^2. The surfaces of the samples were cleaned using a sequence of rinses in acetone, IPA and DI water which were alternated with drying in a stream of nitrogen gas. A 7 µm thick layer of AZ 4562 resist was then spin coated onto the underside of the samples followed by baking in a vacuum oven at 90 °C for 20 min. Lithographic patterning was used to define a circular (5 mm in diameter) or rectangular recess in the resist with dimensions of either 5 x 5 mm^2 or 10 x 15 mm^2. The patterned window in the resist was transferred into the layer of SiC by reactive ion etching (RIE) in a Plasma Sciences system. The RIE process for etching of SiC has consisted of CF_4 gas (50 sccm) at an rf power of 100 W and a base pressure of ~70 mTorr to give an etch rate of 0.02 $\mu m.min^{-1}$. Using the SiC pattern as a mask, the underlying Si wafer was then chemically etched in KOH (45%) solution at a bath temperature of 80 °C. The wafers were suspended in the solution without agitation. An etch time of ~28 hrs was required to fully remove the thickness (650 µm) of Si at 80 °C. After cleaning of the sample in acetone, an array of circular TLM patterns [4] was fabricated onto the surface of the membrane by a standard lift-off process. A layer of AZ1512 resist was spin-coated onto the surface of the membrane and lithographically patterned in a circular TLM structure [4]. As illustrated in Fig. 1, the spacings between electrodes were $r_1' - r_o = 50$ µm and $r_2' - r_1 = 100$ µm. A number of different contact systems including Al (300 nm), Pd (300 nm), Ni (50 nm)/ Ti (50 nm)/ Au (100 nm) and were examined as an ohmic contact to n^+-SiC. Prior to the deposition of metal layers by electron beam evaporation, the patterned samples were dipped in buffered HF solution for 60 sec and rinsed in de-ionised water. The annealing of the contacts and membranes was performed in a nitrogen atmosphere at temperatures up to 950 °C.

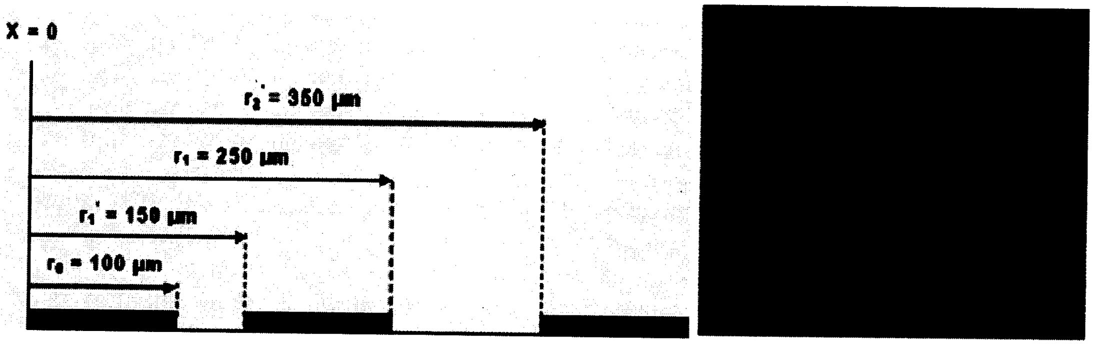

Figure 1. Geometry and dimensions of electrodes in the Circular TLM pattern used in the measurement of specific contact resistance [4].

RESULTS AND DISCUSSION

The membranes were fabricated in a range of sizes up to 10 x 15 mm^2 (Fig.2) in all three thicknesses (0.285, 0.95 and 1.18 μm) of n$^+$-SiC film. However, the thinnest membranes (0.285 μm) were always perforated during the final drying in the stream of nitrogen, even with minimal flow rate of the gas. As a consequence, the remainder of this work has focused on the properties of the thicker (0.95 and 1.18 μm) membranes. For these films, the membranes were fabricated in a circular (5 mm diameter) or rectangular geometry (5 x 5 mm^2 and 10 x 15 mm^2) using the same basic technique. Fig. 3(a) shows the upper surface of a circular membrane with an array of CTLM patterns. The array has extended across the surface of the membrane and on the surrounding wafer. The etched underside of a membrane is shown in Fig. 3(b).

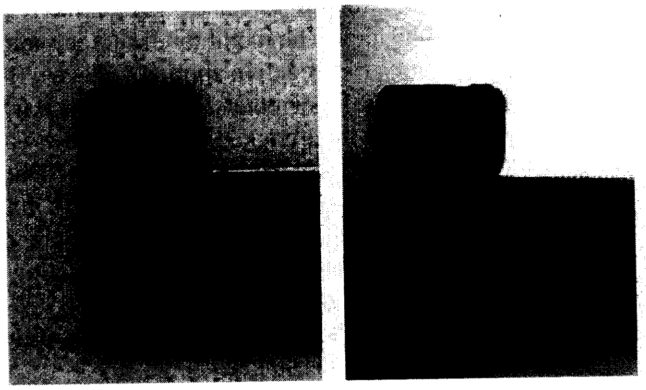

Figure 2. Examples of SiC membranes with dimensions of 5 x 5 mm^2 and 10 x 15 mm^2.

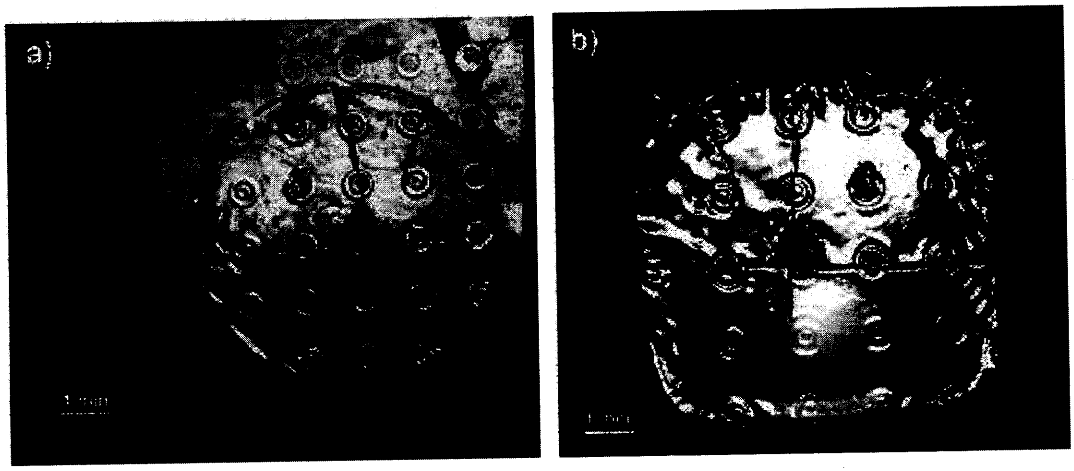

Figure 3. a) Ni/Ti/Au metallization on the upper surface of a 0.95 μm thick membrane, b) the underside of a membrane in which the etched recess was coated with a resin layer.

Annealing of the Pd contacts at 600 °C and Ni/Ti/Au contacts at 950 °C was performed without damage to the membranes. A further critical step in the process was the deposition into the etched recess on the backside of the membrane of a layer of resin. The resin was cured at room temperature for 24 hours. The stiffness of the layer of hardened resin has enabled the mechanical stabilization of the membrane for subsequent probing on the upper surface. The application of the resin was the last step in the fabrication process and followed directly either the metal deposition or annealing of the contacts.

Measurements were performed using the CTLM patterns for each of the metal contact systems. In each case, the as-deposited contacts located on the membranes were ohmic in current/ voltage response. Figure 4(a) shows the linear plot for as-deposited Al contacts. Fig. 4(b) and (c) have compared the current/ voltage plots for Pd (annealed at 600 °C, 5 mins) and Ni/Ti/Au contacts (annealed at 950 °C, 5 mins), respectively. For both the Pd and Ni/Ti/Au contacts, the CTLM contacts located on the membrane have shown an ohmic I/V response. The patterns located on the n^+-SiC/Si substrate outside of the membrane were non-ohmic with a divergence from linearity in I/V response evident at negative applied voltages. Both Pd and Ni/Ti/Au contacts on the n^+-SiC/Si substrate have shown the same divergence from ohmic behaviour. For the CTLM patterns located on the membrane, the current flow was restricted through the metal/ n^+-SiC contact interfaces and within the n^+-SiC/ layer as illustrated in Fig. 5. For CTLM patterns located outside of the membrane, the significant increase in the measured current indicates a current path through the SiC – Si heterojunction and into the conducting Si substrate (Fig. 5). In this case, the increased current flow through the conducting Si substrate has resulted in a decrease in the measurements of resistance.

The specific contact resistance, ρ_c, was determined from measurements of the resistance between inner and outer rings (R1 and R2) and end resistance [7].

$$\rho_c = [\ln(r_2'/r_1)R1 - \ln(r_1'/r_0)R2]\ (r_0)2\Delta \qquad (1)$$

$$\Delta = 2\pi/(\alpha r_0)2\Phi.(A(r_1,r_1')B(r_1,r_1')/C(r_1,r_1') + D(r_1,r_1')^{-1} \qquad (2)$$

where A,B,C and D are combinations of the modified Bessel functions of the first and second kind. The average value of ρ_c was calculated for the Ni/Ti/Au contacts on the membranes as 1.5 x 10^{-4} Ω.cm^2 and for Pd contacts as ρ_c = 2 x 10^{-4} Ω.cm^2.

This value of ρ_c for Ni/Ti/Au contacts to n-SiC was almost the same as ρ_c determined by Barda et al. using a linear TLM pattern on semi-insulating substrate at a doping level of 1.9 x 10^{19} cm^{-3} [9]. Other studies of Ni/n-SiC contacts have measured values of ρ_c within the range 5 x 10^{-6} Ω.cm^2 to 3.47 x 10^{-3} Ω.cm^2. It should be noted that these results were obtained for n-SiC with 4H and 6H poly-type faces [5]. Annealing at temperatures in the range 900-1,000 °C has been shown as necessary for the formation of ohmic contacts based on Ni [5]. At these temperatures, the predominant interface structure has been identified as Ni_2Si and carbon phases [10]. Pd-based contacts have previously been examined as an ohmic contact to p-SiC [5]. Annealing at 600 °C has given a minimum in ρ_c associated with the formation of an interfacial phase of Pd_3Si [11]. The present results indicate that Pd contacts also have the ability to form ohmic contacts to highly doped n-SiC. An advantage of the Pd contacts is the lower temperature of annealing (600 °C) than required to reduce the value of ρ_c for Ni contacts (900-1,000 °C).

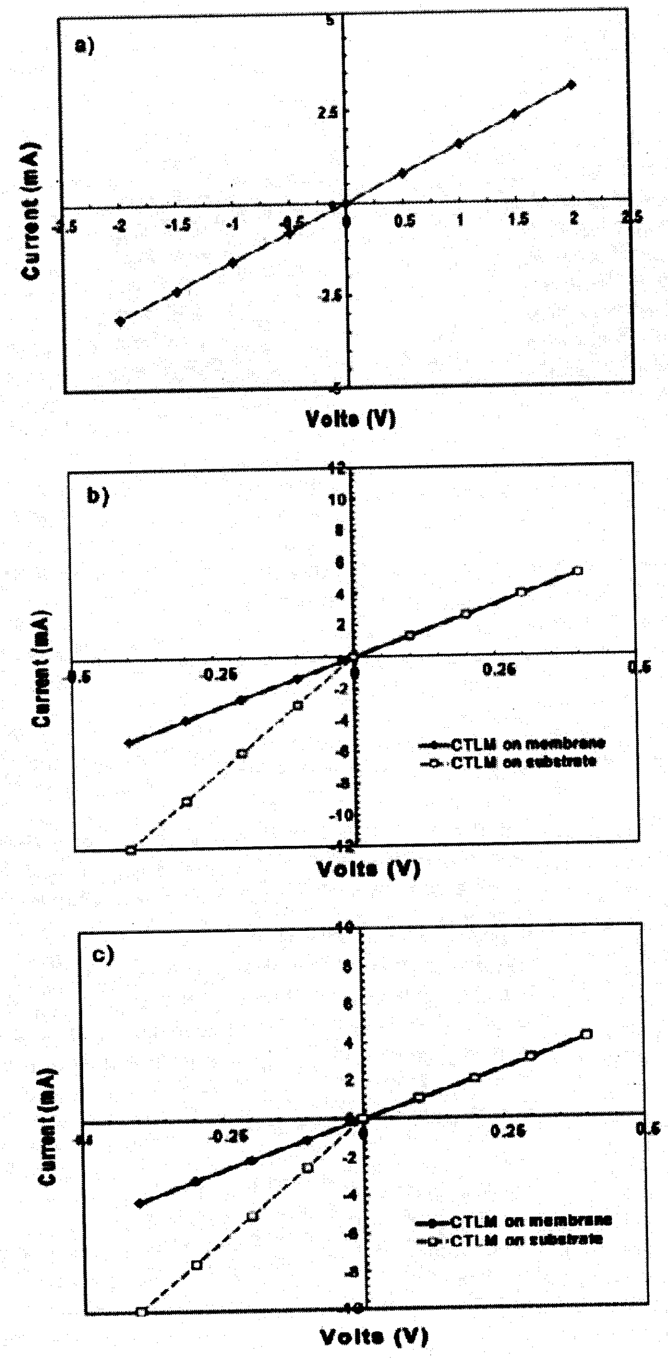

Figure 4. Current-voltage plots for a) Al (300 nm) as-deposited on membrane b) Pd (300 nm) annealed at 600 °C, 5 mins on membrane and on substrate and c) Ni (50 nm)/Ti (50 nm)/Au annealed at 950 °C, 5 mins on membrane and on substrate.

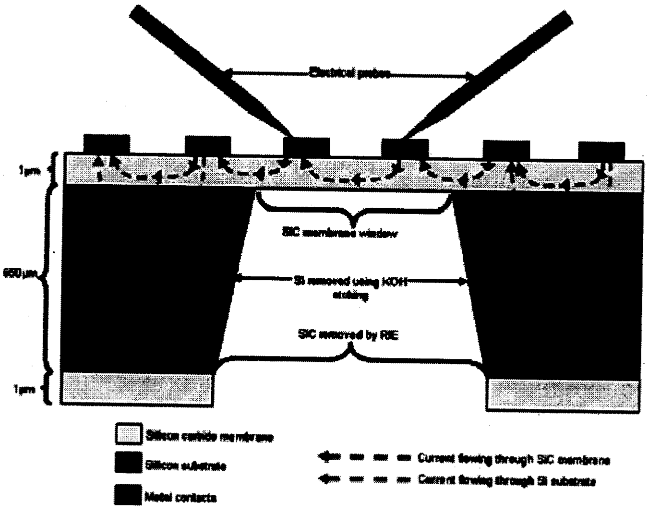

Figure 5. Schematic illustration of the membrane showing the alternate current paths for contacts located on the membrane and on the n^+-SiC/Si substrate.

CONCLUSIONS

1. Membranes with dimensions up to 10 x 15 mm^2 have been fabricated in n^+-SiC epitaxial films.
2. Arrays of circular TLM patterns have been lithographically patterned onto the surface of the membranes and onto the surrounding n^+-SiC film directly over the Si substrate.
3. A layer of resin applied onto the recessed side of the wafer has been used to stiffen the membrane to enable mechanical probing of the upper surface.
4. The CTLM patterns fabricated on the membranes have provided an ohmic current-voltage response with $\rho_c = 1.5 \times 10^{-4}\ \Omega.cm^2$ for Ni/Ti/Au contacts and $\rho_c = 2 \times 10^{-4}\ \Omega.cm^2$ for Pd.
5. The CTLM patterns located on n^+-SiC/ Si substrate have shown a non-ohmic I/V response indicating a significant effect of the Si substrate in increasing current flow between the contacts.

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