Characteristics of small-signal capacitances of silicon-on-sapphire MOSFETs

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Characteristics of small-signal capacitances of silicon-on-sapphire MOSFETs

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The measured inter-electrode capacitances of silicon-on-sapphire (SOS) MOSFETs are presented and compared with simulation results. It is shown that the variations of capacitances with DC bias differ from those of bulk MOSFETs due to change in body potential variation of the SOS device resulting from electron-hole pair generation through impact ionisation.

Introduction: The main difference between silicon-on-insulator (SOI) MOSFETs (of which the silicon-on-sapphire (SOS) device is a subclass) and bulk MOSFETs is that the former has an isolated body. While such a structure has many inherent advantages such as reduced junction capacitances and immunity to CMOS latch-up, it suffers from the effects of a floating body which can significantly affect the device electrical characteristics under high drain fields [1]. The effect of impact ionisation on the DC drain current is well documented but not the small-signal parameters of the device. With the device size shrinking, the effects of impact ionisation on the DC and AC characteristics are more pronounced. In this Letter we present experimental and simulation results of small-signal gate-to-drain (C_{gd}) and gate-to-source (C_{gs}) of an SOS device and highlight the effect of impact ionisation.

Device and method: Partially depleted SOS n-channel transistors with 0.5 μm drawn length, 10 nm gate oxide fabricated on 100 nm thin film silicon were used to investigate the effects of impact ionisation. C_{gd} and C_{gs} were measured against drain and gate bias using an HP 4284A LCR meter. DC characteristics were also measured using a semiconductor parameter analyser. The effect of impact ionisation on device characteristics was studied theoretically by numerical simulation of the test device with and without impact ionisation physics using the 2-D device simulator SILVACO [2].

Results: For a bulk device in inversion, $C_{gs} = C_{gd} = 0.5C_{gate}$ at $V_{ds} = 0$ V, where C_{gate} is the total gate capacitance ($=C_{ox}$.WL). As V_{ds} increases, C_{gs} rises towards to 2/3 C_{gate} and C_{gd} decreases towards zero [3]. Fig. 1 shows the measured C_{gs} and C_{gd} against V_{ds} for the 0.5 μm-length SOS n-MOSFET at $V_{gs} = 1$ V ($V_T = 0.7$ V). C_{gs} rises with increasing V_{ds} but reaches a plateau at $V_{ds} = 0.25$ V and then rises again after 1.2 V. C_{gd} decreases with increasing V_{ds} initially but shows a small peak at $V_{ds} = 1.6$ V before decreasing again. The plot of I_d–V_{ds} at $V_{gs} = 1$ V for the device is also shown in Fig. 1. It can be seen that the features of C_{gs} is closely aligned with the rapid rise in drain current at the onset of impact ionisation [4] at $V_{ds} = 1.2$ V. Impact ionisation induces a forward bias on the body-to-source junction and hence lowering of threshold voltage and an increase in inversion carrier concentration at the source end of the channel. Theory of MOSFET gate capacitances shows that this leads to increase in C_{gs} and a concomitant decrease in C_{gd} [3]. We attribute the observed increase in C_{gs} to this effect. The peaking at $V_{ds} = 1.6$ V and delayed decrease in C_{gd} require explanation. To investigate this, two-dimensional device simulation of the measurement was carried out. For simplicity, we used a uniformly doped substrate and step junctions for the source and drain. The simulation capacitances with and without impact ionisation physics (with SILVACO default parameters for the Selberherr model [2]) are shown in Fig. 2. It is clear that the presence of impact ionisation gives rise to C_{gs} and C_{gd} with the same characteristics, including the detailed structures described, as our measurement. As indicated above, C_{gs} can be understood in terms of impact ionisation induced injection of electrons from source into the channel.

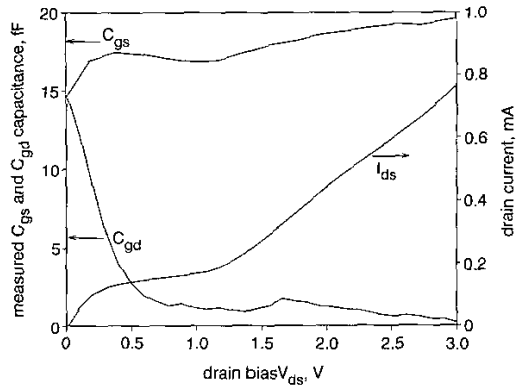

Fig. 1 *Measured C_{gs}, C_{gd} and drain current against V_{ds} of $W/L = 20/0.5$ μm SOS n-MOSFET at $V_{gs} = 1$ V*

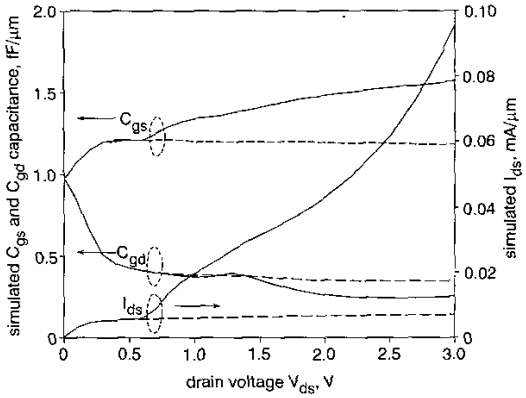

Fig. 2 *Simulated per unit width C_{gs}, C_{gd} and drain current against V_{ds} of $L = 0.5$ μm SOS n-MOSFET at $V_{gs} = 1$ V*

—— with impact ionisation
------ without impact ionisation

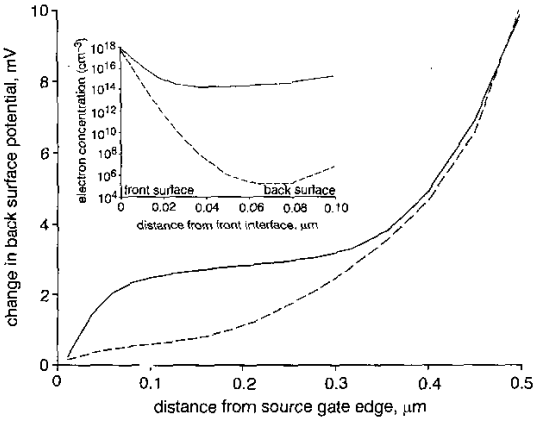

Fig. 3 *Simulated change in back surface potential of SOS n-MOSFET at $V_{gs} = 1$ V and $V_{ds} = 1.4$ V in response to 10 mV change in V_{ds}*

Inset: Mid-channel electron concentration profile
—— with impact ionisation
------ without impact ionisation

To understand the behaviour of C_{gd}, we simulated and plotted in Fig. 3 the change in back surface potential of the SOS transistor with

and without impact ionisation physics in response to 10 mV change in V_{ds} at $V_{ds} = 1.4$ V. This emulates the measurement of C_{gd}. It is seen that impact ionisation leads to higher changes in back surface potential than without impact ionisation. This implies that in measurement the potential of the isolated body is varying in response to the AC signal applied to the drain; this, in turn, leads to a change in electric field across the gate oxide which is detected as an additional component of C_{gd} not seen when impact ionisation is absent. This extra capacitance gives rise to the observed peaking and delayed decrease in C_{gd}. This difference in back surface potential has its origin in impact ionisation induced back surface inversion of SOI devices [5]. That this is indeed the case is seen in the insert in Fig. 3 showing the mid-channel electron concentration profile at $V_{ds} = 1.4$ V and $V_{gs} = 1.0$ V.

At higher V_{ds}, higher impact ionisation rate leads to a stronger inversion channel at the (grounded) source end which electrostatically shields any drain-induced body AC potential from the gate as well as reducing the fraction of C_{gate} that is coupled to the drain. Consequently C_{gd} decreases with increasing V_{ds} as observed. The second-order effect of AC voltage induced impact ionisation suggested by Flandre [6] would reduce C_{gd} further.

Conclusion: We have presented experimental characteristics of the small-signal capacitances of the short-channel SOS MOSFET and attributed, by numerical simulation, the results to impact ionisation and back surface inversion.

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Enhancement-mode p-HEMT using selective hydrogen treatment

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A simple novel enhancement-mode p-HEMT has been fabricated using a selective hydrogen treatment. The DC and RF characteristics of the enhancement-mode p-HEMT, with a threshold voltage of ~0.26 V and $I_{DSS} \cong 0.9$ mA/mm, show a selective hydrogen treatment is an effective method to implement an enhancement operation of any HEMT structure without degradation of DC and RF performance except the linearity.

Introduction: Enhancement-mode HEMTs (E-HEMTs) have attracted increased interest recently as a solution to various requirements including single power supply in hand-held telephone power amplifiers and a direct-coupled FET logic necessary to implement high-speed, low-power digital PLL, DA converter, frequency divider, and decision circuits as building blocks of fibre optic communication systems [1]. To date, most E-HEMTs have been implemented by reducing the gate-to-channel distance through a double recess process [2] or increasing the Schottky barrier height [3]. However low etch selectivity or poor adhesion of gate metal has made it difficult to fabricate E-HEMTs using these methods. A novel process overcomes these disadvantages by employing a selective hydrogen treatment (SHT) in the gate region of the HEMT structure without any further recess etching and any use of different Schottky metal.

Previous work found that the SHT technique had considerable effects on device characteristics including threshold voltage shift, transconductance, gate leakage current and low-frequency noise characteristics [4]. These changes are mostly related to the passivation of donor impurity and defects, and the change of surface stoichiometry [5]. Using the SHT technique and taking advantage of large threshold shift, we implemented monolithic integration of E/D-HEMTs more easily without degradation of transconductance and RF performance.

Device fabrication: A commercially available $Al_{0.24}Ga_{0.76}As/In_{0.2}Ga_{0.8}As$ double heterostructure p-HEMT epi-wafer was used for the experiment (see Fig. 1). Devices were isolated by forming a mesa by means of wet etching with phosphoric-based etchant and ohmic contacts were formed by evaporating Ni/Au/Ge/Ni/Au and annealing at 405°C for 20 s. The gate recess was carried out using citric-based etchant while monitoring the current. The hydrogen treatment consists of two steps: (i) hydrogen exposure using RIE and (ii) annealing at 470°C for 25 s under N_2 atmosphere. The samples underwent identical processing except for the hydrogen treatment and RTA. During the hydrogen treatment, the samples were masked with photoresist except for the gate region (2 μm) to prevent degradation of ohmic characteristics. After hydrogen treatment, Ti/Pt/Au gate metal (2 μm) was deposited, followed by Si_xN_y device passivation and deposition of pad metal for probing.

Results and discussions: Basically the selective hydrogen treatment controls the threshold voltage by changing only the concentration of the activated donor under the cross-hatched gate region as shown in Fig. 1, unlike other techniques which adjust the Schottky barrier height or the gate-to-channel distance to produce sufficient shift in threshold voltage. The threshold voltage of p-HEMTs can be expressed as:

$$V_T = \Phi_B - \frac{\Delta E_C}{q} - \int_d \int \frac{qN_D(x)}{\varepsilon} dx^2 \quad (1)$$

where Φ_B is the Schottky barrier height, ΔE_C is the conduction band discontinuity, N_D is the activated donor concentration, and d is the thickness of the barrier layer. While ΔE_C and d are intended to be invariant for various RF power and RTA temperature conditions, Φ_B and N_D are ascribed to such a large threshold voltage shift. As the RF power of hydrogen plasma increases, more atomic hydrogens are generated in the RIE chamber, accelerated by the electric field, and diffused into the gate region. The diffused hydrogen atoms neutralise Si donors as well as deep-level defects near the surface and in the bulk. However, the electrical reactivation of the silicon donors can be obtained up to >90% after thermal treatments at temperatures >450°C for silicon-doped AlGaAs treated by hydrogen plasma, while deep levels are still passivated for temperature <600°C [6]. Therefore the proper thermal annealing recovered DC characteristics of a device to such an extent and simultaneously makes the residual deactivated donors in the barrier layer still serve to shift the threshold voltage to the positive direction as shown in (1). Table 1 shows the threshold voltage V_{TH}, the gate-grounded drain current I_{DSS}, the cutoff frequency f_T and the maximum oscillation frequency f_{max} for various RF power conditions under the thermal annealing at 470°C. Fig. 2 shows the transconductance and the drain saturation current characteristics of the D-HEMT and the E-HEMT processed by SHT with RF power of 100 W. Fig. 3 shows the RF performances of the D-HEMT and the E-HEMT, which were measured at the bias condition exhibiting the peak g_m. The Figures suggest that a large shift in the threshold voltage of the HEMT can be achieved without degradation of transconductance and RF performance by changing RF power of hydrogen plasma through the SHT technique. However, the SHT technique causes degradation in the linearity of the p-HEMT as shown in Fig. 2 since the neutralisation of donors produces reduction of free electron concentra-