The Design of Tag-ItTM Compatible 13.56 MHz Passive RFID Transponder IC Employing TSMC 0.18µm Process

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Abstract: - This paper presents the design of Tag-It™ compatible 13.56 MHz Passive RFID Transponder IC implemented in TSMC 0.18µm Mixed Signal SALICIDE (1P6M, 1.8V) process. The design is simpler and requires lower power supply, compared to four other works, which in turn can achieve power reduction of 30 - 50%.

Key-Words: - Transponder, RFID, Low power

1 Introduction

Throughout the years, several works had been published in the open literature for the IC design for 13.56MHz range passive transponders. Work by Masui, S et al. [1] sees the realization of a read/write transponder, which includes anti-collision and authentication, all controlled by a CPU for power compensation. Using the same type of rectification as previously used by a team of smartcard designers [2], Panitantum, N et al. [3] designed a read only passive transponder optimized for a very low power operation. It employs a zener-zap one-time programmable ROM to store the ID and an anti-collision scheme. All the mentioned works use the ASK modulation scheme and are implemented in the 0.8µm CMOS process. Another work by Villard, P et al. [4] is a mixed-mode CMOS/SOI RFID chip, the first of its kind. Supply voltage of 1.2V for the digital part and 1.5V for the analog part was achieved using the 0.25µm partially-depleted CMOS/SOI technology. Although this technology played a good role in lowering the required voltages of the functional transponder, a more common CMOS process is used in this paper, as it is easily available in low cost.

Our work use TSMC 0.18µm Mixed Signal SALICIDE (1P6M, 1.8V) process, a newer technology from the existing works [1][3][5], resulting in smaller die size and layout area. We follow the Texas Instrument's Tag-It™ protocol for compatibility. We use simpler circuits, but achieving the same level of requirement expected for RFID passive transponder. Our design requires lower power supply, compared to three other works [1][3][5], which in turn can achieve power reduction of 30 – 50%.

2 Architecture

Figure 1 shows our architecture, based on [3], but using the TSMC 0.18µm technology and following the Tag-It™ protocol. The system can be divided into two modules. Analog modules consist of the full wave rectifier, voltage regulator, load modulator, clock extractor and frequency divider while the encoder and ROM make up the digital modules.

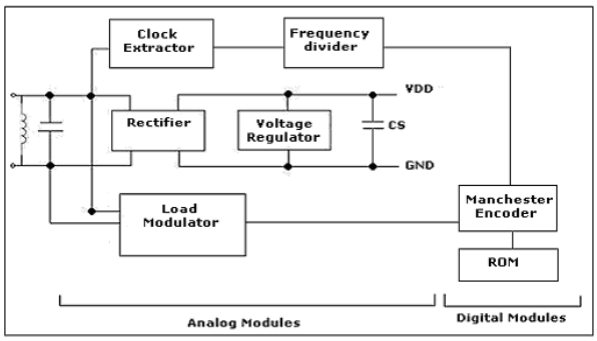

Fig. 1 Block diagram of the transponder

The system works in half duplex. The analog modules extract the power from the incoming RF signal and convert it through a full wave rectifier to be stored in C_S. This stored charge will then be used to power the entire chip. The system clock is directly extracted from the incoming RF signal. The digital modules transmit the Manchester encoded data back to the reader using load modulator with subcarriers of 423.75 kHz and 484.28 kHz.

3. Building Blocks

3.1 Rectifier

A PMOS bridge rectifier [2][3], rectifies the RF signal from the LC tank to the voltage regulator and also charges up C_S. PMOS is chosen as an approach to a simpler structure and also to avoid the existence of a latch-up as its floatable n-well alleviate the substrate bias.

3.2 Voltage Regulator

Voltage regulator regulates the voltage supplied from Cs and to provide a constant DC voltage of 1.8V. The non-regulated voltage, Vrec generated from the rectifier is fed into the input of the voltage regulator. The voltage regulator is known as the series pass regulator [5], as shown in Figure 2. It consists of 3 major parts. Operational amplifier is used as the two-stage error amplifier. R1 and R2 are used as resistive voltage divider. A series pass transistor M1 forms a current amplifier. The operational amplifier consists of 2 stages. The first stage consists of a differential amplifier while the second stage is a single stage common source amplifier. M4 and M5 are used to form the differential pair input of the differential amplifier. M6 and M7 act as the active load of the differential amplifier. M3 provides the biasing current by mirroring the current from external current source to drive the differential amplifier. The second stage acts as gain stage and output stage, consisting of a common-source-connected transistor M8. M2 provides biasing current to the single stage amplifier and acts as the active load at the same time. C2 is used to accomplish the Miller compensation or to performed frequency compensation, which in turn to provide stability.

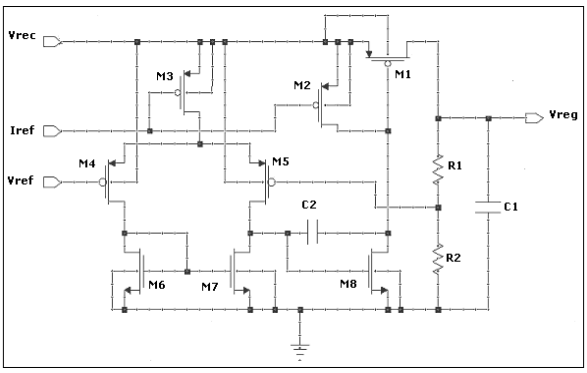

Fig. 2 Voltage regulator

Vref and Iref provide 0.6V and 1μA respectively for the error amplifier. Iref is generated using a self-biasing current source circuit, comprising of a basic current mirror and Widlar current source. The Widlar current source is chosen to produce low biasing current where normal current mirror cannot achieve.

3.3 Clock Extractor

The clock extractor [3] is designed from a Schmitt trigger inverter. The RF signal is used as the input clock. Clock extractor converts the RF sine wave to a 13.56MHz full square wave with the short rise and fall times independent of the varying input signal amplitude. These square wave pulses with a constant VDD of 1.8V serve as the clock source for the digital modules.

3.4 Frequency Divider

To deliver a subcarrier of 423.75 kHz and 484.29 kHz, a divide-by-32 frequency divider and a divide-by-28 divider are constructed respectively.

3.5 Memory

A 128-bit ROM is constructed in the 16 x 8 = 128 bit matrix. The NOR ROM topology is chosen to implement the 1 and 0 ROM cells. It uses PMOS load to pull up the bit lines when none of the attached NMOS devices is enabled. To read the ROM content, a row and a column index decoder are designed. The 128-bit of data will then be encoded using the Manchester encoder.

3.6 Data Encoder

Tag-It™ protocol specifies that the Manchester high bit and low bit takes 8 RF cycles and 9 RF cycles respectively to transmit. Manchester high bit has a typical duration of 18.88μs and Manchester low bit takes 18.54μs. The total bit length is 37.42μs.

3.7 Load Modulator

The transmission of the data back to the reader is achieved using a capacitive load modulator [2][3] as shown in Figure 3. C1 and C2 are switched on and off in time with the encoded data. This will vary the resonance frequency of the transponder and causes it to switch between two frequencies. The transmission of Manchester high level is represented by 423.75

kHz while the Manchester low level is represented by 484.29 kHz.

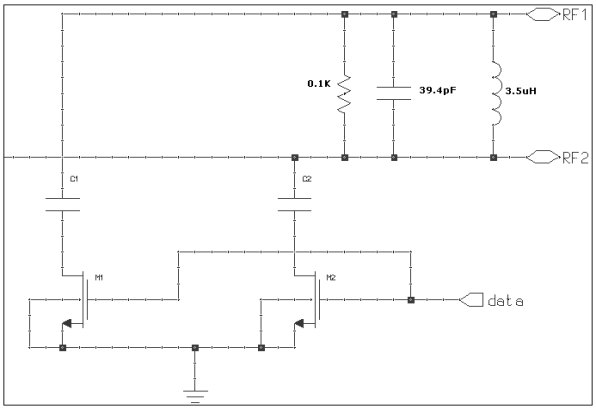

Fig. 3 Load modulator

4 Results and Discussion

The PMOS bridge rectifier shows C_S being charged up to 7V within 300µs. For the voltage regulator, it is capable of keeping a constant DC voltage of 1.8±5% when the input voltage from the rectifier ranges from 7V to 3V. Meanwhile, the clock extractor demonstrates a good square wave of 13.56MHz. Figures 4 and 5 respectively show the Manchester encoding for the NRZ data bits and load modulation using the two subcarriers. Load modulation using subcarriers ideally differentiates useful signals from noise.

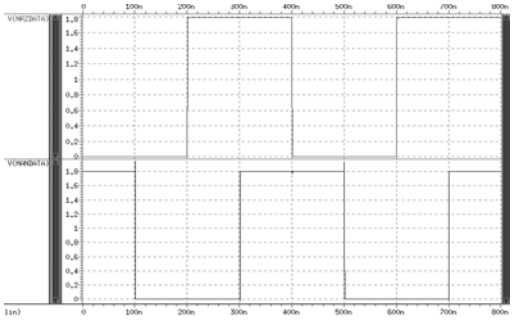

Fig. 4 Manchester encoding

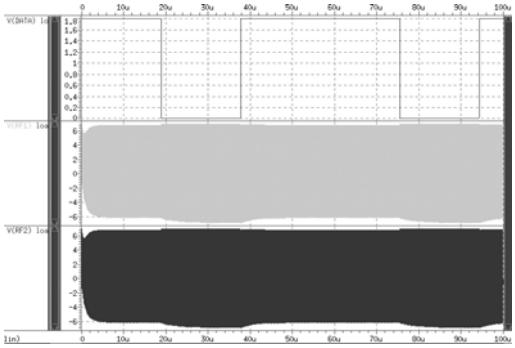

Fig. 5 Load Modulation

Table 1 shows the comparison of our design to the transponders designed by four other works, also working on the carrier frequency of 13.56MHz. Our design has smaller dimension technology, which is 0.18µm and also lower power supply of 1.8V and has 30 –50% power reduction, compared to the works by Panitantum, N et al. (0.8µm, ~3.5V), Masui, S. et al. (0.8µm, 2.6V) and C.C.Tsai et al. (0.35µm, 3V). The work by Villard, P et al. using the 0.25µm partially depleted CMOS/SOI technology has the edge in lowering the power supply to 1.2V for digital parts and 1.5V for analog parts. However, the fabrication and packaging cost is higher compared to TSMC 0.18µm. We also make our design compatible with Texas Instruments Tag-IT^{TM} protocol.

5 Conclusion

The design of 13.56MHz RFID transponder has been presented. The design specification is compatible with Texas Instrument Tag-It protocol. A state-of-the-art TSMC 0.18 micron technology is employed. The performances are compared to four other previous works. It is found that this design is simpler, and could achieve a power reduction of 30-50%, while maintaining the same specification. The next work is to integrate ESD protection circuitry to increase the robustness of this system.

References:

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Table 1 Comparison of works

	This project	Panitantum, N et al. [3]	Masui, S et al. [1]	P.Villard et al. [4]	C.C.Tsai et al. [5]
Technology	TSMC 0.18µm 1P6M Salicide	0.8µm 2P2M CMOS	0.8µm CMOS	0.25µm partially depleted CMOS/SOI	TSMC 0.35µm 1P4M Silicide
Power supply	1.8V	~3.5V	2.6V	1.2V (digital), 1.5V (analog part)	3V
Modulation type	Load modulation with subcarriers of 423.75 kHz (RF/32) and 484.29 kHz (RF/28)	Load modulation with subcarrier of 423.75 kHz (RF/32)	BPSK with subcarrier frequency of 847.5 kHz (RF/16)	DQPSK with 212 kHz subcarrier (RF/64)	BPSK with subcarrier frequency of 847.5 kHz (RF/16)
Bit representation	Manchester	Manchester	NRZ	-	NRZ