Threshold-free localized scheme for DC fault identification in multiterminal HVDC systems

Threshold-free Localized Scheme for DC Fault Identification in Multiterminal HVDC Systems

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***Abstract*— In the future grid scenario, the continuous operation of large-capacity remote power transmission over an augmented DC network is imperative for implementing a reliable multi-terminal high voltage direct current (MT-HVDC) grid or, alternatively, an MTDC grid. A fast and selective DC fault identification method with improved reliability eventually enhances the operational continuity and flexibility of the MTDC grid. Based on the *V/I* ratio of a current limiting reactor, this paper proposes a new non-unit protection scheme for DC fault identification without a threshold value setting. The DC fault is precisely identified in a span of three sampling intervals by the *V/I* ratios of four sampling instants. The selectivity of the proposed scheme is verified in a four-terminal MTDC grid. Simulation results demonstrate that the effective detection, discrimination, and location of a DC fault strictly satisfies the speed requirement (<1ms) with a location error of less than 1%. Moreover, the relevant sensitivity analyses reveal that the proposed scheme remains invariant for a wide range of fault locations and resistances and perform efficiently, even with a lower sampling frequency. In addition, transient events apart from DC faults fail to trigger the protection, indicating the high robustness of the proposed scheme.**

***Keywords*—DC reactor, fault location, fault resistance, multi-terminal DC (MTDC) grid, non-unit scheme, selective protection.**

I. INTRODUCTION

WITH the immense development of modular multilevel converter (MMC) technology, the multi-terminal high voltage direct current (MT-HVDC) system, often referred to as an MTDC system offers a promising alternative for integrating large-scale renewable sources and interconnecting asynchronous power grids [1], [2]. Reflecting that, the first ever four-terminal MTDC grid is constructed in Zhangbei, China with MMC's of ±500kV/3000MW [3]. The reliability of an MTDC grid broadly relies on the continuous operation of the DC grid with an effectual protection scheme [4]. In a few milliseconds after a DC fault, the low-impedance DC path results in an enormous fault current feed by multiple MMCs and might damage the power electronic components [5]. Taking the Zhangbei MTDC grid as an example, a minimum 3-ms fault detection time is required to interrupt a maximum possible fault current of 25kA [3], [6]. Moreover, the ambiguous fault transient could trigger a maloperation of the DC breaker in a more complex MTDC network. Therefore, fast, selective, and reliable fault identification is crucial for implementing an effective MTDC grid.

In selective protection, a DC circuit breaker (DCCB) is used to isolate the faulty line from the healthy grid following a tripping signal from the fault protection scheme. In general, two types of selective schemes, i.e., unit and non-unit protection schemes are available in the literature. Despite the problem associated with time delays, the unit protection schemes proposed in [7]-[9] may improve the selectivity. A unit protection scheme based on the cosine distance criterion is reported in [7]. This method is susceptible to the time delay of long-distance lines. A pilot protection scheme is presented in [8] using the wavelet transform-based current travelling wave. The authors in [9] proposed an upgraded protection scheme based on the differential voltage traveling wave considering the frequency-dependent line model. However, the unit protection methods proposed in [8], [9] are challenging to implement due to complex computations and long protection times. Moreover, the unit protection scheme requires communication links between two or more measuring points. Therefore, it is convenient to use as back-up protection.

The non-unit scheme is employed as the primary protection scheme with stringent requirements including high-speed detection. A summary of the non-unit protection methods is provided in Table I. Based on the travelling wave and transient signal; several non-unit protection schemes have been reported in the literature [10]-[15]. Adopting the concept of travelling wave, a frequency spectrum-based protection scheme is proposed in [10]. Although this scheme can provide rapid detection, it requires a higher sampling frequency to implement. A protection algorithm is developed in [11] with a relatively lower sampling frequency and the positive sequence component of the voltage travelling wave. However, the external transient components might jeopardize the robustness of the scheme proposed in [11]. A transient voltage-based protection scheme is proposed in [12] to ensure greater robustness by extracting the high-frequency components of the line voltage using

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TABLE I
SUMMARY OF THE NON-UNIT PROTECTION METHODS

Ref.	Protection speed	Sampling frequency	Computational complexity	Threshold search	Fault resistance Impact
[10]	High (< 1ms)	Higher (2MHz)	High	Required	Low
[11]	High (< 1ms)	High (20 kHz)	High	Required	Low
[12]	Relatively low (> 1ms)	High (20 kHz)	High	Required	Low
[13]	High (< 1ms)	Higher (200 kHz)	High	Required	Low
[14]	Relatively low (> 1ms)	Low (10 kHz)	Higher	Required	Low
[15]	Relatively low (> 1ms)	High (50 kHz)	Higher	Required	Low
[16], [17]	High (< 1ms)	Lower (< 10 kHz)	Low	Required	Low
[18]	High (< 1ms)	High (20 kHz)	Low	Required	Low
[19]	High (< 1ms)	Lower (< 10 kHz)	Low	Required	Low
[20]	High (< 1ms)	Lower (< 10 kHz)	Low	Required	Low
[21]	High (< 1ms)	Lower (< 10 kHz)	Low	Required	Low
Proposed method	**High (< 1ms)**	**Lower (1~10 kHz)**	**Low**	**No Threshold**	**No impact beyond safety margin**

wavelet transform. However, the protection speed is relatively low for the proposed scheme in [12]. Nevertheless, the travelling wave-based localized scheme suffers from a low-sensitivity problem. This is further improved in [13] by the Levenberg-Marquart (LM) optimal approximation method. With better sensitivity, median absolute deviation (MAD)-based statistical method in [14] and high-frequency model-based frequency domain method in [15] are proposed to detect the transient fault signal. However, the high computational burden associated with the model in [14] and [15] makes them difficult to realize practically for large MTDC systems.

To simplify the computation process, various non-unit protection methods have been proposed based on the voltage, current, and their derivatives [16]-[21]. Due to poor selectivity, under-voltage [16] and over-current [17]-based protections are less dominant than the derivative-based method. With a greater selectivity, current derivative-based high-speed protections are reported in [18], [19]. The common mode (CM) and differential mode (DM) based current derivative method in [18] is relatively fast with a lower sampling frequency. However, the robustness of the proposed scheme was not properly justified in [18]. Despite better robustness, time-interval selection is difficult for a large MTDC grid in [19]. Moreover, the reactor-based voltage derivative methods reported in [20] and [21] are sensitive to intense noise and fault resistances.

The aforementioned high-speed localized schemes can improve the selectivity with the provision of threshold value settings. However, the estimation of threshold value is a challenging task and requires high computations with a systematic search. For example, in [12], [14] numerous fault events with repetitive simulations are needed to look for the critical set-points of threshold values. Moreover, the threshold settings are largely affected by the variation of system parameters, fault resistances, and so on [14]. Furthermore, despite improving the selectivity, the higher threshold value results in a reduced sensitivity and eventually impairs the reliability of the protection scheme.

To address the issues outlined above, a novel threshold-free localized scheme is proposed in this paper with enhanced speed and reliability. Based on the *V/I* ratio of a current limiting DC reactor, an algorithm is developed to detect, discriminate, and locate the DC fault effectively.

In particular, the contributions and novelties of the proposed scheme are outlined as follows:

1) A fast, simple, and novel protection method based on the "*V/I* ratio" of the DC reactor.
2) Unlike existing protection methods, no threshold search is required.
3) Sense any fault resistance beyond the safety margin.
4) Simultaneously detect, discriminate, and locate a DC fault with better selectivity, sensitivity, and robustness.

The rest of the paper is organized as follows. The *V/I* ratio of the current limiting reactor is formulated as the key index for the DC protection scheme in Section II. Section III presents the proposed method of the overall protection scheme including the detection, discrimination, and location criteria. The test system and the comprehensive simulation results are presented in Section IV. The sensitivity and robustness of the proposed scheme are evaluated in Section V and Section VI, respectively. Finally, Section VII concludes the findings of the paper.

II. MATHEMATICAL OVERVIEW

To enhance the reliability of a DC breaker, a DC reactor is used in an MTDC grid as shown in Fig. 1(a) to limit the rising rate of the fault current in case of fault contingency. The DC reactor provides a high impedance path in the DC grid and acts as a boundary for the high frequency transient signals caused by the DC fault [20]. In this article, the ratio of the reactor voltage and current, more precisely, the *V/I* ratio of the DC reactor is employed as the basic index for the proposed protection scheme. For representing the "*V/I* ratio" and the "change in *V/I* ratio", the symbols of "X" and "ΔX" are successively employed throughout the paper.

A. Fault Detection Principle

In a normal state, the voltage developed across the reactor is approximately zero [19] and the current through the reactor remains steady. Therefore, the DC reactor does not experience any significant reactance value. Hence, in the pre-fault stable state, the *V/I* ratio of a DC reactor is expressed as:

$$X_{st} = V_R / I_{DC} \approx 0 / I_0 \approx 0 \quad (1)$$

where V_R is the reactor voltage and $I_{DC} = I_0$ is the steady-state DC current.

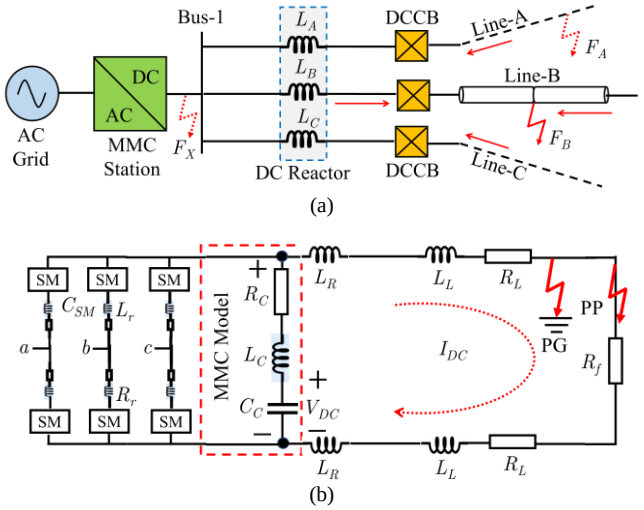

Fig. 1. An MMC-HVDC system with DC fault dynamics: (a) Single-ended MTDC grid with multiple DC reactors; (b) Equivalent model.

After the occurrence of a DC fault, a non-sinusoidal transient signal is developed, which causes the capacitive energy of the DC grid to release rapidly through the fault. Consequently, the reactor voltage and current increased rapidly that results in a higher *V/I* ratio in the DC reactor. From the simplified equivalent model of an MMC-HVDC system as shown in Fig. 1(b), the fault dynamics of the DC grid is mathematically presented as [22]:

$$(R_C + aR_L)I_{DC} + (L_C + bL_R + aL_L)\frac{dI_{DC}}{dt} = V_{DC} - V_f \qquad (2)$$

where the MMC components are denoted as the resistance R_C = $2R_r/3$, inductance L_C = $2L_r/3$, and capacitance C_C = $6C_{SM}/N$. The arm resistance R_r, arm inductance L_r, and N number of sub-modules are also defined in each arm with C_{SM} capacitance. Moreover, the fault-resistance drop is V_f, the DC reactor value is L_R, and the fault path resistance and inductance values are represented by R_L and L_L, respectively. Furthermore, the integer value a is 1 and 2 for a pole to ground (PG) and pole to pole (PP) fault, respectively. Due to series of two converters with a neutral grounding in bipolar MMC, the values of R_C and L_C are considered half during a PG fault. The analysis is explained further in subsection B with Fig. 2. The integer value b varies based on the internal and external DC faults as discussed in the next section.

Since the resistive drop in the transient state is trivial, the post-fault DC current evaluated from (2) is represented as:

$$I_{DC} = I_0 + \left(\frac{1}{L_T}\right)\int_{t_0}^{t}(V_{DC} - V_f)dt \qquad (3)$$

where the total inductance value of the fault discharging path is denoted as $L_T = L_C + bL_R + aL_L$.

It is evident from (3) that the DC current (I_{DC}) is inversely proportional to V_f or, more specifically, the fault resistance R_f. Therefore, a large value of fault resistance eventually decreased the DC current and might fail to reach the threshold value for an overcurrent (ΔI) or current derivative (dI/dt)-based protection scheme. Moreover, a protection scheme relating to the DC voltage i.e., under-voltage (ΔV) or voltage derivative (dV/dt)-often suffers from grid-oriented threshold settings, as described in Section I. Hence, the ratio of reactor voltage and current is utilized to define a *V/I* ratio of the DC reactor and establish a threshold-free protection scheme.

In the transient state, the DC reactor value is represented by

$$X_{tr} = \frac{L_R\left(\frac{dI_{DC}}{dt}\right)}{\left[I_0 + \left(\frac{1}{L_T}\right)\int_{t_0}^{t}(V_{DC} - V_f)dt\right]} \qquad (4)$$

For the DC reactor, the change (increase) of *V/I* ratio after the fault event is determined from (1) and (4), as follows:

$$\Delta X = \frac{L_R L_T\left(\frac{dI_{DC}}{dt}\right)}{\int_{t_0}^{t}(V_{DC} - V_f)dt} \qquad (5)$$

From the above analysis, it is worth noting that the post-fault *V/I* ratio of the DC reactor is noticeably higher than the pre-fault *V/I* ratio. This characteristic eventually develops the basis of the proposed fault detection criteria.

B. Fault Discrimination Principle

For analyzing the fault discrimination criteria, internal fault F_B and external faults F_X, and F_A are incepted at multiple locations of the MTDC grid as shown in Fig. 1(a). The line-B protection unit at bus-1 side is considered to be the reference protection scheme for the DC fault discrimination. For simplification, only a single (positive) pole DC line is taken into consideration, and the inductance value in line-A and line-B are assumed to be equal.

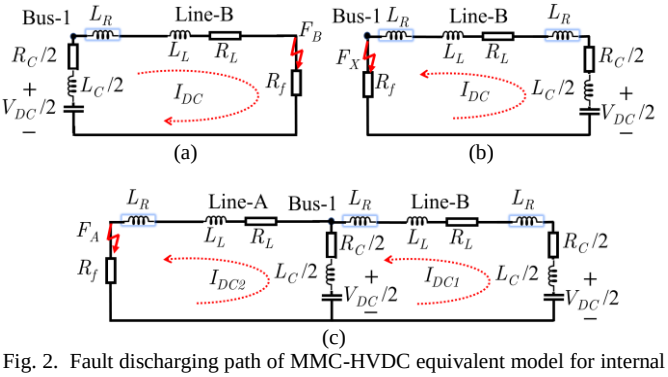

Fig. 2. Fault discharging path of MMC-HVDC equivalent model for internal and external DC faults: (a) F_B (internal) line fault; (b) F_X (external) bus fault; (c) F_A (external) line fault.

The post-fault discharging path for the given faults are depicted in Fig. 2. The total inductance value of the fault discharging path for the internal line fault, external bus fault, and external line fault are successively described as follows:

$$L_{Tb} = L_R + L_L + (L_C/2) \qquad (6)$$

$$L_{Tx} = 2L_R + L_L + (L_C/2) \qquad (7)$$

$$L_{Ta} = 3L_R + 2L_L + (L_C/2) \qquad (8)$$

The expressions in (6)-(8) reveal that the total inductance value of the fault discharging path exhibits a substantial difference for internal and external DC faults. For example, the value of b is 1, 2, and 3 for F_B, F_X, and F_A faults, respectively. Therefore, an external fault causes higher inductance value in the fault discharging path. Moreover, for a particular R_f, the rising of *V/I* ratio largely depends on the inductance term (L_RL_T) as evident from (5).

Hence, in general, (5) can be expressed as

$$\Delta X \infty L_T \qquad (9)$$

where other variable terms (I_{DC} and V_f) in (5) mostly rely on L_T for a particular R_f. The large L_T value causes a reduced I_{DC} and eventually results in a higher value of ΔX. Therefore, for the internal and external DC faults, the basis of the fault

discrimination criteria is developed using (9) and can be represented as follows:

$$\frac{\Delta X_X}{\Delta X_B} = \frac{L_{Tx}}{L_{Tb}} = 1 + \frac{L_R}{L_{Tb}} = \alpha \quad (10)$$

$$\frac{\Delta X_A}{\Delta X_B} = \frac{L_{Ta}}{L_{Tb}} = 1 + \frac{(2L_R+L_L)}{L_{Tb}} = \beta \quad (11)$$

where ΔX_X, ΔX_A, and ΔX_B are the change of *V/I* ratio for external bus fault, external line fault, and internal line fault, respectively.

This is apparent from (10) and (11) that the change of *V/I* ratios for external bus fault and line fault are successively α and β times greater than the internal DC fault, where $\alpha = 1 + \left(\frac{L_R}{L_{Tb}}\right)$ and $\beta = 1 + \left[\frac{(2L_R+L_L)}{L_{Tb}}\right]$. Moreover, the value of β is significantly higher than α (i.e., $\beta > \alpha$). Hence, considering a unity change of *V/I* ratio for an internal DC fault (i.e., $\Delta X_B = 1\Omega$), the maximum change of *V/I* ratio for an external DC fault (ΔX_X or ΔX_A) is found to be β. Therefore, the change of *V/I* ratio for an external DC fault is formulated as

$$\Delta X_{ext} \leq \beta . \Delta X_{int} \quad (12)$$

$$\Delta X_{ext} \leq \left(1 + \frac{(2L_R+L_L)}{L_{Tb}}\right) \quad (13)$$

where, $\Delta X_{ext} \in \{\Delta X_X, \Delta X_A\}$ and $\Delta X_{int} \in \{\Delta X_B\}$.

However, instead of unity change consideration, the change of *V/I* ratio for an internal DC fault can be more précised by considering the safety margin of the post-fault *V/I* ratio and thereby ΔX_{int} is expressed as

$$\Delta X_{int} = X_{SM} \quad (14)$$

Henceforth, (12) can be re-written as follows:

$$\Delta X_{ext} \leq \left(1 + \frac{(2L_R+L_L)}{L_{Tb}}\right) X_{SM} \quad (15)$$

Consequently, the rate of rising (ΔX value in Δt time) of the *V/I* ratio for an external fault shows distinct characteristics (slow rising) compared to an internal DC fault. Hence, this criterion can be utilized in the protection scheme to discriminate the DC faults (internal and external).

Based on the principle stated above, the DC fault identification technique with an exemption of the conventional threshold value is adopted in this paper.

III. Proposed Protection Scheme

In an MTDC grid, the non-unit protection units (PUs) are usually embedded in both sides of the DC line [4]. The continuous sampling of voltage and current sensor measurements in PUs are closely monitored to actuate the proposed protection scheme, described in this section.

A. Fault Detection Criteria

In a pre-fault steady-state condition, the voltage across the DC reactor is nearly zero [19]. Hence, at the pre-fault ($t = t_{-1}$) and fault ($t = t_0$) instant, the respective reactor values are:

$$X_{-1} = X_0 = V_0/I_0 \approx 0 \quad (16)$$

In the transient state succeeded by a DC fault event, the *V/I* ratio of the DC reactor rises abruptly and reaches to a higher value. Therefore, at the post-fault instant $t = t_1$, the DC reactor value is expressed by

$$X_1 = V_1/I_1 \quad (17)$$

where X_1 is a large value of the post-fault *V/I* ratio depends on the fault transient components. Moreover, to ensure a reliable tripping decision, one more measurement is sampled at $t = t_2$ instant and the respective *V/I* ratio of the DC reactor is presented as follows:

$$X_2 = V_2/I_2 \quad (18)$$

Therefore, in total, four sampling values (X_{-1}, X_0, X_1, and X_2) and three sampling intervals ($\Delta t_0 = [t_0 - t_{-1}]$, $\Delta t_1 = [t_1 - t_0]$, and $\Delta t_2 = [t_2 - t_1]$) are required to formulate the basic criteria for the fault detection. Furthermore, to limit the signal ripples and measurement noises in practical systems, low pass filters are utilized. A sufficient safety margin (0.1 p.u.) is considered for the fault detection scheme [21]. Hence, in general, the triggering and the detection criteria are successively expressed as follows:

$$Cr-1:\ (|X_i| - |X_{i-1}| > X_{SM}) \wedge (|X_{i-2}| - |X_{i-1}| < X_{SM}) \quad (19)$$

$$Cr-2:\ |X_i - X_{i-1}| \geq |X_i - X_{i+1}| \quad (20)$$

where $i = 1$ is the first sampling value (present sample) just after the DC fault, and the safety margin of the *V/I* ratio is X_{SM} =50 Ω. When the criteria mentioned in (19) and (20) are sequentially satisfied, the DC fault is successfully detected.

B. Fault Discrimination Criteria

Following a successful detection of the DC fault, the fault types are explicitly distinguished using the fault discrimination criteria described in this section. These criteria are verified to identify two types of DC faults: 1) internal and external faults 2) PG and PP faults.

1) *Internal and external DC faults:* A DC fault incepted within the protection zone of the respective DC line is defined as an internal fault, while a fault outside of the protection zone is called an external fault [5]. For example, in Fig. 1(a), the PU for line-B detects the DC fault F_B as an internal fault and identify F_X, and F_A as the external DC faults. To differentiate these faults, the post-fault *V/I* ratio samples of the DC reactor are used in the proposed protection scheme.

For an internal DC fault, the respective reactor voltage rises immediately due to a quick decay of the DC line voltage [20]. Moreover, the reactor current rises accordingly considering the fault line impedance. Consequently, for an internal fault, the post-fault *V/I* ratio sample reaches to a higher value and starts declining from its peak almost instantly.

On the contrary, an external DC fault causes a smaller DC line current with a reduced reactor voltage and results in a slow rising *V/I* ratio. Subsequently, the sample of *V/I* ratio for an external DC fault takes longer time to reach its peak value compared to an internal DC fault. Hence, following a DC fault the ΔX value in Δt time is employed to discriminate the DC fault. Therefore, based on the discrimination principle stated in the previous section, the internal and external DC fault discrimination criteria are prescribed as follows:

$$\text{Cr-3: } \textit{Fault Type} = \begin{cases} Int., & if \ \frac{|X_i - X_{i-1}|}{(t_i - t_{i-1})} > \left(1 + \frac{(2L_R + L_L)}{L_{Tb}}\right) X_{SM} \\ Ext., & otherwise \end{cases} \quad (21)$$

2) *PG and PP faults:* After the identification of an internal fault, the respective DC protection scheme differentiates the fault as a PG or PP fault. The change of *V/I* ratios from X_0 to X_1 in two consecutive sampling instants (sampling interval $\Delta t_1 = [t_1 - t_0]$) referred as the slope of *V/I* ratio ($\Delta X/\Delta t$) is used to discriminate the faults. Hence, the measurement of $\Delta X/\Delta t$ value does not require any time derivative block. The slopes of the *V/I* ratio in the paired (positive, *p* and negative, *n*) pole DC reactors are almost identical for a PP-type DC fault. Therefore, the slope difference in the paired poles is nearly 0 (zero). Conversely, for a PG fault, only the faulty pole (positive or negative) DC reactor shows a higher *V/I* ratio slope, which results in a unity (approximately) slope difference in the paired poles. Hence, the discrimination criteria for PG and PP faults can be reported as follows:

$$\text{Cr-4:} \qquad \text{Fault Type} = \begin{cases} PP, & if \ 0 \le \frac{|S|}{A} \le k_{PP} \\ PG, & if \ k_{PG} \le \frac{|S|}{A} \le 1 \end{cases} \quad (22)$$

In (22), the subtraction and addition factors of the paired-pole *V/I* ratio slopes are defined as, $S = \{(\Delta X_p/\Delta t) - (\Delta X_n/\Delta t)\}$ and $A = \{(\Delta X_p/\Delta t) + (\Delta X_n/\Delta t)\}$, respectively. Moreover, considering a deviation of 0.1p.u. from the ideal slope difference, the upper and lower limit safety margin for PP and PG faults are successively defined as k_{PP}=0.05 and k_{PG}=0.8, respectively [21].

C. Determination of Fault Location

From the single-ended (non-unit) measurement data, a DC fault location is determined using the lumped π-type equivalent model of a DC overhead line (OHL). This article employs the OHL model reported in [23], where a detail frequency dependent transmission line is modelled using a simplified RL representation. In order to ease the computational complexity, OHL π-model is largely utilized for DC fault transients and protection studies [19], [23], [24].

The OHL π-model is approximated as a series *RL* circuit with ample accuracy considering the following assumptions [19], [24]-[26]: 1) travelling wave phenomena is neglected, 2) length of the OHL is less than 250km, 3) a higher order OHL π-section, i.e., 10 is used, and 4) OHL capacitance (~10^{-2}μF) is insignificant compared to MMC capacitance (~10^{2}μF) and thereby, ignored. It is worth noting that the fault location estimation with the aforementioned assumptions is merely feasible for a single-ended protection scheme. However, an exact assessment of the DC fault location without considering the assumptions must require communication links with unit protection schemes.

Figure 3 illustrates the paired poles of a DC OHL with a lumped value of resistance *r* and inductance *l* in per unit length. A PP fault with R_f fault resistance is incepted on the DC line. The length of the fault location from the measurement point is *D*. For the positive and negative pole pair, the measurement point potentials are $+V_a$ and $-V_d$, and the fault location potentials are $+V_b$ and $-V_c$, respectively. The current through the positive and negative poles are I_{ab} and I_{cd}, respectively. To reduce the computational burden, single-ended measurements are taken excluding the DC reactor. Hence, only the transmission line parameters are considered to compute the fault location.

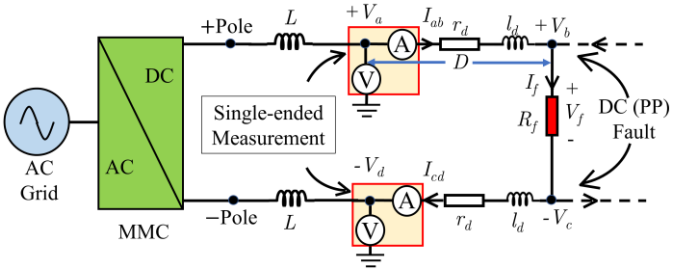

Fig. 3. Single-ended measurement for DC fault location identification.

Applying *KVL* to the positive and negative pole pair, (23) and (24) are formulated respectively and expressed as follows:

$$V_a - V_b = r_d I_{ab} + l_d \left(\frac{dI_{ab}}{dt}\right) \quad (23)$$

$$V_d - V_c = r_d I_{cd} + l_d \left(\frac{dI_{cd}}{dt}\right) \quad (24)$$

The potential difference across the fault resistance can be written as:

$$V_b + V_c = I_f R_f = V_f \quad (25)$$

Thereafter, (25) is used following the addition of (23) and (24) altogether to get the fault location *D* as follows:

$$D = \frac{V_a + V_d - V_f}{r(I_{ab} + I_{cd}) + l\left(\frac{dI_{ab}}{dt} + \frac{dI_{cd}}{dt}\right)} \quad (26)$$

In (26), all the parameters of the right-hand side are readily achieved from the single-ended measurement point except the voltage drop across the fault resistance (V_f). If R_f is negligible enough, then V_f=0. Therefore, considering $V_a = V_d = V$, and $I_{ab} = I_{cd} = I$, (18) can be expressed as follows:

$$Cr-5: \qquad \text{D} = \frac{V}{\left[rI + l\left(\frac{dI}{dt}\right)\right]} \quad (27)$$

However, an increasing value of V_f in (26) is compensated by the reduction of the denominator current values accordingly and thereby, the fault location *D* remains unaffected. A similar study can be performed for a PG fault, which produces the same expression given in (27) and effectively be utilized for locating the PG fault. The DC line parameters are computed off-line through the fault test method as described in [23].

D. Overall Protection Scheme

For the identification of a DC fault, no threshold setting is required in the proposed protection scheme. A window of four consecutive samples is sufficient to identify (detection, discrimination, and location) the DC fault. The window of sampling sequences and the flowchart of the complete protection scheme are shown in Fig. 4 and 5, respectively.

After every instant of sampling, the respective sample value is passed through some simple and quick computational blocks to check for the identification criteria discussed previously.

For triggering the scheme, the present i^{th} sample value of *V/I* ratio is compared with the preceding $(i - 1)^{th}$ value and the *Cr*-1 (triggering) criterion is examined for $(i - 1)^{th}$ and $(i - 2)^{th}$ sample values at every instant. Following a successful triggering of the protection scheme, the detection of the DC fault is verified by

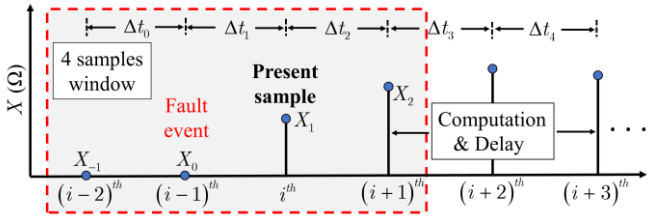

Fig. 4. Sampling sequences with a data window for DC fault identification.

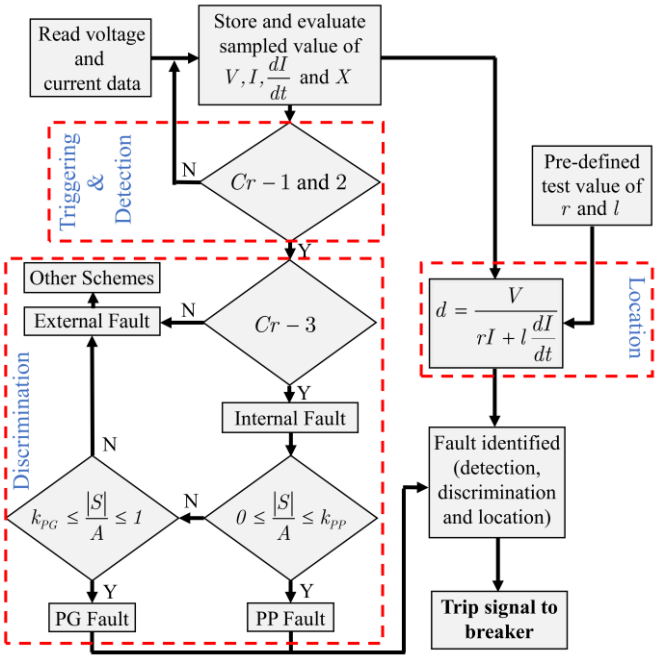

Fig. 5. Flowchart for a threshold-free protection scheme.

comparing the present i^{th} sample value of *V/I* ratio with the preceding $(i - 1)^{th}$ and succeeding $(i + 1)^{th}$ value and the detection is finalized when the criterion *Cr*-2 (detection) is fully satisfied. Hence, a DC fault is successfully detected with the *V/I* ratios of three sampling intervals (Δt_0, Δt_1, and Δt_2).

For discriminating the detected DC fault, the same *V/I* ratios of i^{th} and $(i - 1)^{th}$ sample are taken into consideration to verify the *Cr*-3 criterion. Hence, internal, and external DC faults are effectively discriminated after satisfying the *Cr*-3 criterion. Moreover, using the same sampling information of Δt_1 interval, the *V/I* ratio slope for the discrimination (PG and PP) and current slope for the location are explicitly determined.

In brief, after the fault event at $t = t_0$ instant, four samples of the *V/I* ratio value (X_{-1}, X_0, X_1, and X_2) in three sampling intervals (Δt_0, Δt_1, and Δt_2) are required to properly identify a DC fault.

Considering relevant delays, all the computational tasks are executed within the span of two sampling intervals (Δt_3 and Δt_4) as shown in Fig. 4. Following the detection of the DC fault after Δt_2 interval, the protection algorithm uses the previous sampling values to discriminate and locate the fault, simultaneously. Hence, the computational delay is negligible; therefore, the protection scheme is quite fast.

IV. Simulation Results and Validations

This section broadly analyses the overall protection schemes through non-linear simulations to validate the feasibility of the proposed method.

A. Test System

A four-terminal MMC-based HVDC grid as shown in Fig. 6 is adopted in this paper as the test system. The simulation model is developed in DIgSILENT PowerFactory [27], and the parameters are provided in Table II. In the given test system, MMC-1 station regulates the DC voltage to balance and continue the grid power support ($V_{DC}Q$ - mode), while MMC-2, 3 and 4 stations are operated to control the active and reactive power flow (*PQ* - mode). To realize the selective fault detection, a current limiting reactor is employed at every single end of a DC line. The sampling frequency is selected as 10kHz. In order to minimize high frequency components, the measurement signals are passed through a first-order lag filter with a unity gain and 0.001s of the process time constant.

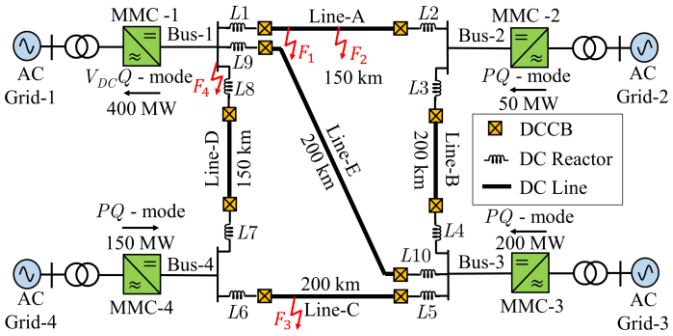

Fig. 6. A four-terminal MMC-based HVDC grid.

TABLE II
Parameters of the MTDC Grid

System Parameters	Value	System Parameters	Value
Rated AC voltage, kV	275.5	SM capacitance (C_{SM}), mF	15
DC voltage (V_{DC}), kV	±500	Arm inductance (L_r), mH	60
Rated DC current, kA	2	Arm resistance (R_r), Ω	0.006
Transformer reactance, p.u.	0.15	DC line resistance (r), Ω/km	0.011
Rated MMC capacity, MVA	500	DC line inductance (l), mH/km	0.519
SMs per arm (N)	200	DC reactor (L_R), mH	100

B. Fault Identification Performance Analysis

To verify the identification performance of the proposed protection scheme, several DC faults are simulated sequentially at different locations of the test system as shown in Fig. 6. Unless specified, all the faults are applied at 0.1s with a fault resistance of 10Ω. With the sampled value of reactor voltage and current, the *V/I* ratio of the respective reactor is continuously computed and checked by the PU to identify the DC fault.

1) *Detection:* To detect a DC fault, the system in Fig. 6 is subjected to a PG fault on the positive pole of line-A located at 15km (10% fault distance) from bus-1. The output responses of the voltage, current and *V/I* ratio values of the nearest DC reactor (*L*1) are outlined in Fig. 7. It is ascertained from Fig. 7 that the negligible reactor voltage in the pre-fault steady-state

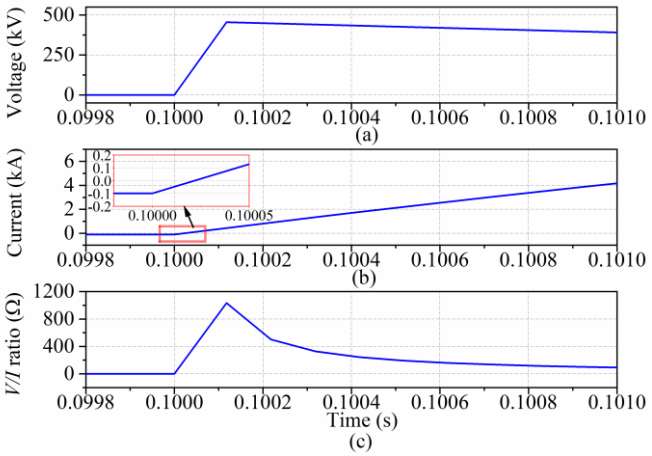

Fig. 7. Single-ended measurement of $L1$ reactor for DC fault detection: (a) Reactor voltage; (b) Reactor current; (c) Reactor *V/I* ratio.

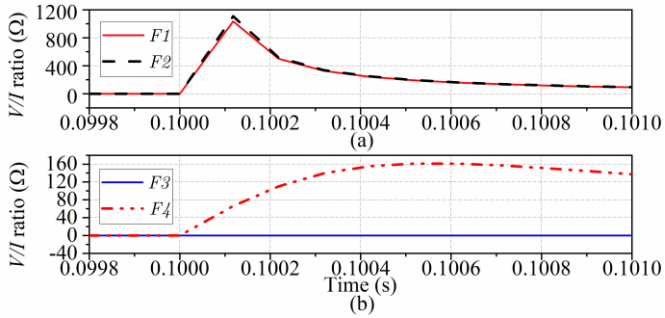

Fig. 8. *V/I* ratio of $L1$ for DC fault discrimination: (a) Internal fault; (b) External fault.

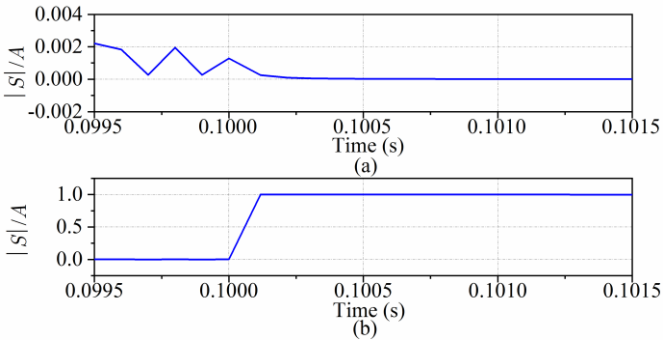

Fig. 9. $|S|/A$ factor of $L1$ for DC fault discrimination: (a) PP fault; (b) PG fault.

results in a *V/I* ratio of 0.0012Ω, which acts like a short circuit. Moreover, the post-fault *V/I* ratio prompts a significantly larger value of 1034Ω almost instantly and rapidly decays to its pre-fault steady-state condition. Therefore, the post-fault *V/I* ratio value is considerably higher than the pre-fault value, which necessarily validates the basic principle of the proposed scheme.

From Fig. 7(c), it is also apparent that in two successive sampling intervals on fault application, the changes of *V/I* ratios (ΔX) are found to be 1034Ω and 532Ω, respectively. Hence, the ΔX value exceeds the safety margin (1034Ω > 50Ω) in the first interval and is deemed to be smaller (532Ω < 1034Ω) in the second interval and onwards. Furthermore, the value of ΔX is almost negligible (0.00011Ω < 50Ω) in the pre-fault sampling interval. Therefore, all the criteria of fault detection (Cr-1 and Cr-2) are fully satisfied, and a fault is successfully detected in the DC grid.

2) *Discrimination:* After detecting the DC fault, the type of the fault is discriminated as an internal or external fault using the post-fault *V/I* ratio values. For the PU of a specific line segment, an internal fault is further discriminated into a PG or PP fault. From the system parameter given in Table II, the value of β is computed as 2.4 and the value of βX_{SM} = 120Ω.

a) Internal and external fault discrimination: To differentiate the internal and external DC fault, four separate PG faults are applied sequentially on four different locations as follows: 1) $F1$: positive pole of line-A at 15km from bus-1, 2) $F2$: at the mid-point of positive pole in line-A, 3) $F3$: positive pole of line-C at 20km from bus-4, and 4) $F4$: at bus-1. The *V/I* ratios of $L1$ relevant to these faults are shown in Fig. 8. The DC fault $F1$ is already detected in the previous section, and hence the PU for line-A is taken as the reference scheme in this section to differentiate the faults mentioned above.

For $F1$ and $F2$ DC faults, Fig. 8(a) reveals that the post-fault rising values of the *V/I* ratio are sequentially decreasing after a few sampling instants until they reach to the pre-fault steady-state values. In case of $F1$ fault, the change of *V/I* ratio for the first sampling interval is found to be 1034Ω, which is higher than the value of βX_{SM}. This eventually satisfies the fault discrimination criterion of *Cr*-3, and thereby, defines the DC fault $F1$ as an internal fault. Similar verification is also valid for $F2$ fault (1106Ω > βX_{SM}) and the respective fault is assigned as an internal DC fault. Due to additional fault line inductance, the rising of *V/I* ratio is slightly higher for $F2$ DC fault.

Figure 8(b) shows the *V/I* ratio values of the line reactor for $F3$ and $F4$ DC faults. It is evident from Fig. 8(b) that the PU in line-A remains non-responsive to $F3$ DC fault. Hence, $F3$ is treated as an external DC fault by the reference protection scheme (PU in line-A). Furthermore, $F4$ DC fault can be effectively detected and discriminated using the post-fault *V/I* ratio samples. Following the DC fault $F4$, the change of *V/I* ratio for the first sampling interval is found to be 65Ω. Hence, the discrimination criterion (65Ω <βX_{SM}) is satisfied for an external DC fault. The rising of *V/I* ratio values is not that much steeper for the external fault $F4$. This is since all the line reactors connected to the bus develop a large value of inductance, altogether and eventually slow down the discharging process.

b) PG and PP fault discrimination: To differentiate the PG and PP fault, the system in Fig. 6 is subjected to a PG (p pole) and PP fault individually on line-A at 10% fault distance from bus-1. From the *V/I* ratio slope, the value of $|S|/A$ is computed for the relevant reactor pair and separately demonstrated in Fig. 9. It is apparent from Fig. 9 that the pre-fault zero value of $|S|/A$ remains unchanged for a PP fault and prompts to unity for a PG fault. Hence, the PG and PP faults are easily discriminated by the proposed method.

3) *Location:* To verify the protection scheme for identifying a fault location, a PG fault is incepted on the positive pole of line-A, located at 15km from bus-1. From the nearby converter station (MMC-1), the single-ended measurement data of the post-fault voltage, current and current slope are found as 35.706kV, 0.44kA, and 4.55kA/ms, respectively. Moreover, the offline resistance and inductance value of the faulty line are computed as 0.01148Ω/km and 0.52003mH/km, respectively using the *RL* model reported in [23]. Therefore, the fault

TABLE III
MEASUREMENT VALUES FOR DC FAULT LOCATION

Fault Type	Sampling Instant (s)	V (kV)	I (kA)	dI/dt (kA/ms)	D (km)	Error (%)
P-G	0.1	499.62	0.0985	0.0001	418569	480
	0.1001	35.706	0.4400	4.5512	15.118	**0.8**
	0.1002	51.259	0.8915	4.4797	22.101	47
P-P	0.1	499.62	0.0985	0.0001	418569	480
	0.1001	36.315	0.4432	4.6317	15.109	**0.7**
	0.1002	43.832	0.9005	4.5539	18.589	24

distance D is calculated as 15.118km, which is approximately equal to the actual fault distance. For a PP fault with the same fault event, an almost similar value of the fault distance is found with a location error of less than 1%.

For PG and PP faults, the computational values of the single-ended measurement are given in Table III. It is noted from Table II that the accuracy of the fault location is higher in the first sampling interval. In the pre-fault state, the absence of the denominator term (di/dt) produces a large D value, which eventually becomes nullified by the criteria of the protection scheme. After the fault event, the sudden appearance of the di/dt term produces a fault location almost equivalent to the actual one. However, the precise location of the DC fault can be assured with the maximum current slope value and the location error increases linearly with the declining values of the current slopes.

V. SENSITIVITY ANALYSIS

The fault characteristics of the DC grid are considerably affected by the fault resistance and location of the fault. Moreover, the sampling frequency might have an impact on the protection of DC faults. This section briefly describes the sensitivity of the proposed protection scheme with these influencing factors.

A. Influence of Fault Resistance

To verify the resistive sensitivity, a wide range of fault resistance (0 ~ 500Ω) is considered for the DC fault and applied at the midpoint of line-A in Fig. 6. The changes in V/I ratios varying with the fault resistance are shown in Fig. 10(a). The gap of post-fault ΔX in two successive intervals (Δt_1 and Δt_2) decreases slowly with the increasing values of fault resistance and thereby, gradually makes a less sensitive protection scheme. However, the value of (X_1-X_0) is far gre ater than the value of (X_1-X_2), even for a large fault resistance of 500Ω (1.7p.u.). Moreover, the value of (X_1-X_0) remains larger than the safety margin for all ranges of R_f. Therefore, without any threshold value, the protection scheme can perform effectively for a wide range of R_f with greater sensitivity.

B. Influence of Fault Location

The test system portrayed in Fig. 6 is subjected to a number of DC faults located at 10%, 30%, 50%, 70%, and 90% length of line-A to verify the fault location sensitivity of the proposed protection scheme. The results delineated in Fig. 10(b) exhibit that the value of (X_1-X_0) remains greater than (X_1-X_2), irrespective of the fault location. Moreover, the post-fault V/I ratio is far greater than the safety margin for all ranges of the fault locations. Therefore, the proposed scheme can identify a DC fault without any threshold value, and the sensitivity of the protection is not altogether affected by the location of the DC fault.

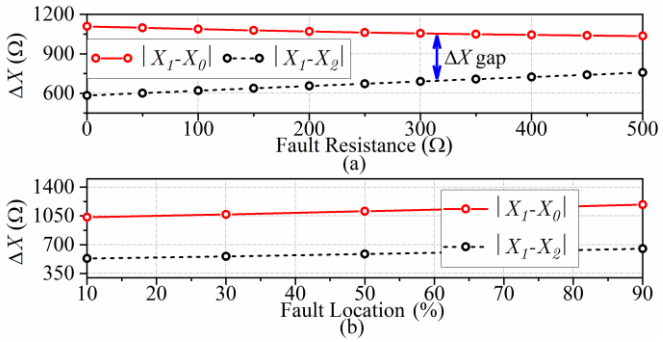

Fig. 10. Sensitivity (change of X) of the protection scheme: (a) Influence of fault resistance; (b) Influence of fault location.

C. Influence of Large R_f (kΩ) with Multiple Fault Inception Instants

In the fault discharging path of a DC grid, the consideration of a large R_f (kΩ) results in a slow rising (or decay) fault current during the transient state [22]. This is characterized in this paper with multiple fault events applied at bus 1 of Fig. 6. The DC faults are incepted at the instants of 0.1s, 0.11s, and 0.12s with R_f values of 1kΩ, 1.1kΩ, and 1.2kΩ, respectively. The V/I ratio of $L1$ reactor following the fault events are shown in Fig. 11. The post fault ΔX values for two successive intervals (Δt_1 and Δt_2) are also given in Table IV. All the protection criteria are

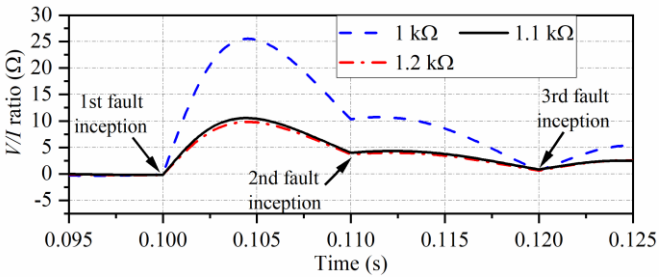

Fig. 11. Sensitivity (change of V/I ratio) of the protection scheme for large R_f (kΩ) values with multiple fault inception instants.

TABLE IV
PROTECTION RESPONSE FOR LARGE R_F (KΩ) WITH MULTIPLE FAULT INCEPTION INSTANTS

R_f (kΩ)	Fault Inception Instant (s)	Sampling Instant (s)	Δt (s)	ΔX (Ω)	Criteria Violation
1.0	0.1	0.0999	-	-	Cr-1
		0.1	Δt_0	0.0098	
		0.1001	Δt_1	1.1725	
		0.1002	Δt_2	0.9952	
1.1	0.11	0.1099	-	-	Cr-1
		0.11	Δt_0	-0.3040	
		0.1101	Δt_1	0.0656	
		0.1102	Δt_2	0.0516	
1.2	0.12	0.1199	-	-	Cr-1
		0.12	Δt_0	-0.1295	
		0.1201	Δt_1	0.1579	
		0.1202	Δt_2	0.1349	

properly satisfied, except the condition of safety margin. Hence, this is evident that the protection scheme can detect all the ranges of R_f values beyond the limit of safety margin.

It is to be noted that a large R_f (kΩ) value can be realized and cleared effectively by a conventional breaker (relatively slow protection) within a reasonable breaking capacity [21]. This is because a large R_f (kΩ) value does not allow the fault current to rise adversely. Moreover, the unit protection scheme is mostly used to sense these large R_f (kΩ) values [7]. Hence, the major concerns of the high-speed protection criteria are not overlooked and a wide range of fault resistances (0~1.7p.u.) are considered for the proposed scheme. For multiple fault inception instants, it is also apparent from Fig. 11 that the proposed scheme performs efficiently without affecting the sensitivity of the protection scheme.

D. *Influence of Sampling Frequency*

The performance of the protection scheme is validated for different sampling frequencies for a DC fault in line-A and the results are given in Table-V. The change in ΔX is higher for higher sampling frequencies without any impact on the sensitivity of the protection scheme. A higher sampling frequency can make the detection faster. However, the proposed protection criteria are fully satisfied, even for a lower sampling frequency (1 kHz). The value of (X_1-X_0) is always greater than the value of (X_1-X_2), irrespective of the sampling frequency. Therefore, the overall proposed scheme is not affected by the sampling frequency.

TABLE V
PROTECTION RESPONSE TO DIFFERENT SAMPLING FREQUENCIES

Sampling Frequency (kHz)	$\lvert X_1\text{-}X_0 \rvert$ (Ω)	$\lvert X_1\text{-}X_2 \rvert$ (Ω)	Change in ΔX (Ω)
1	213.815	108.634	105.181
2	457.622	228.265	229.357
5	1350.376	710.908	639.468
10	3742.597	2253.946	1488.651
20	32519.800	27415.352	5104.448

VI. ROBUSTNESS EVALUATION

A robust protection scheme remains non-responsive to the transient events that are not DC faults. Considering power variation and AC side fault, this section evaluates the robustness of the proposed protection scheme. Moreover, the performance of the proposed scheme is briefly compared with the existing protection methods.

A. *Response to Power Variation*

To verify the response of the protection scheme for grid power variation, the MTDC grid in Fig. 6 is subjected to a power switching event from 0.5 to 0.25p.u for MMC-3 and from 0.38 to 0.18p.u. for MMC-4 at 1s. Moreover, the same switching event in reverse power order is performed at 2s, and the output responses are shown in Fig. 12.

The variation of power results in a transient current in line-E and develops a *V/I* ratio spike at around 1.06s in *L*10 reactor. This exceeds the safety margin. However, ΔX values fail to satisfy the subsequent detection criteria as shown in Table VI.

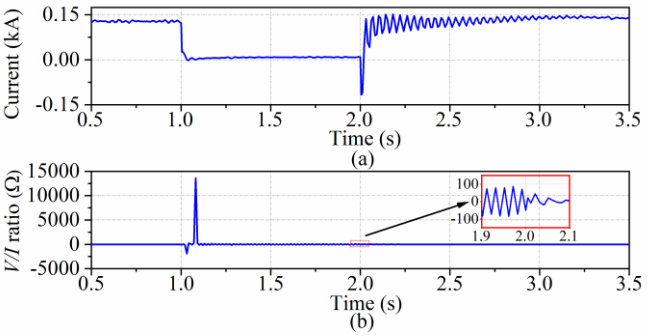

Fig. 12. The DC grid response to power variation in MMC-3 and MMC-4: (a) Current in line-E; (b) *V/I* ratio of *L*10 reactor.

TABLE VI
PROTECTION RESPONSE TO POWER VARIATION

Sampling Instant (s)	ΔX (Ω)	Criteria Violation	Sampling Instant (s)	ΔX (Ω)	Criteria Violation
1.0628	38.355	*Cr*-1	1.0634	2628.24	*Cr*-1
1.0629	56.938	*Cr*-2	1.0635	329.64	*Cr*-1
1.0630	103.44	*Cr*-2	1.0636	133.98	*Cr*-1
1.0631	220.29	*Cr*-2	1.0637	70.336	*Cr*-1
1.0632	845.53	*Cr*-2	1.0638	45.250	*Cr*-1
1.0633	4828.1	*Cr*-1	1.0639	30.502	*Cr*-1

For example, at 1.0630s sampling instant the value of ΔX is 103.44Ω. Despite being higher than the preceding value (56.938Ω), the present ΔX value (103.44Ω) is lower than the following one (220.29Ω) and thus violates the *Cr*-2 detection criterion. Similarly, *Cr*-1 and *Cr*-2 criteria are also violated in different sampling sequences. Therefore, the proposed algorithm does not respond to a power variation event, thus indicating a more robust protection scheme.

B. *Response to AC Faults*

Outside of the DC protection zone, a single-phase short circuit fault is introduced on the AC side of MMC-3 station for 80ms. The value of the *V/I* ratio for *L*10 reactor shown in Fig. 13 reveals that the fault transient quickly reaches to the DC protection scheme and exceeds the safety margin within a few ms. However, the ΔX values shown in Table VII indicate that all other detection criteria are clearly violated to trigger the protection scheme. For example, the preceding ΔX value of 1.0040s sampling instant is above the safety margin (722.09Ω > 50Ω) and thus fails to satisfy the *Cr*-1 (2nd part of *Cr*-1) triggering criterion. This is also true up to the sampling instant

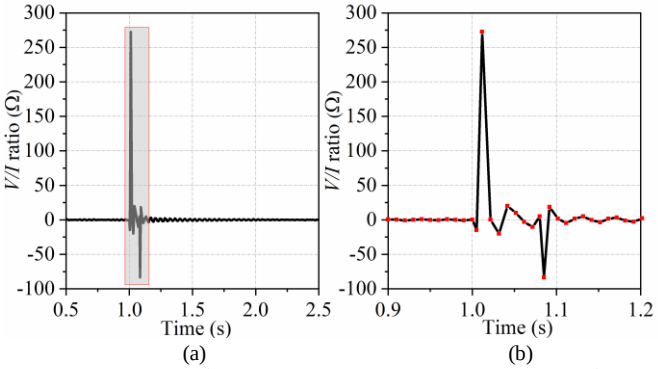

Fig. 13. The *V/I* ratio of L10 reactor in response to MMC-3 AC side fault: (a) Compact view; (b) Enlarged view.

TABLE VII
PROTECTION RESPONSE TO AC FAULTS

Sampling Instant (s)	ΔX (Ω)	Criteria Violation	Sampling Instant (s)	ΔX (Ω)	Criteria Violation
1.0034	25.903	*Cr*-1	1.0040	6980.26	*Cr*-1
1.0035	36.590	*Cr*-1	1.0041	3703.28	*Cr*-1
1.0036	55.752	*Cr*-2	1.0042	368.975	*Cr*-1
1.0037	95.605	*Cr*-2	1.0043	140.119	*Cr*-1
1.0038	202.66	*Cr*-2	1.0044	73.919	*Cr*-1
1.0039	722.09	*Cr*-2	1.0045	45.751	*Cr*-1

of 1.0045s, and all other values do the same for the *Cr*-1 and *Cr*-2 criteria. Hence, the proposed protection scheme is able to overlook the AC fault with greater robustness.

C. Comparison with Existing Methods

In terms of speed, selectivity, and sensitivity, the efficacy of the proposed method is compared with several non-unit protection schemes presented in the literature [12], [18], and [21]. The protection methods based on voltage derivative (*dv/dt*) [12], current derivative (*di/dt*) [18], and reactor voltage (V_R) [21] are precisely dependent on their respective threshold settings.

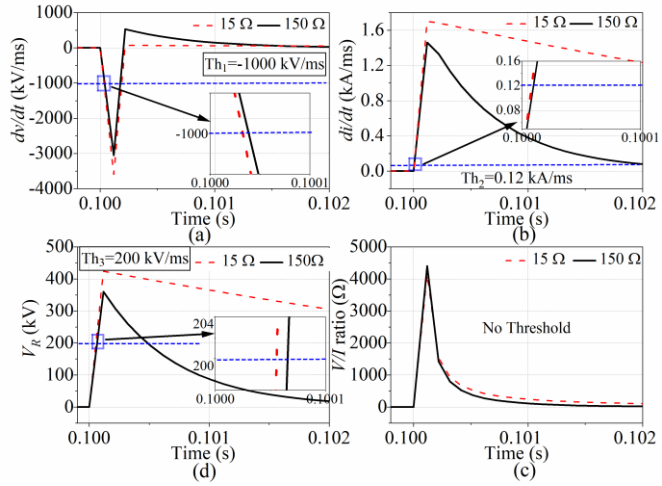

Fig. 14. Responses of various protection schemes for multiple DC faults: (a) *dv/dt* method; (b) *di/dt* method; (c) V_R method; and (d) *V/I* ratio method.

Regarding the speed requirement, all the above-mentioned protection methods are quite fast in fault detection and able to respond within milliseconds. In Fig. 14, the protection responses of the given methods are compared with the proposed method for two separate DC faults. The R_f values are taken as 15Ω and 150Ω, successively. The threshold settings considered for *dv/dt*, *di/dt*, and V_R methods are -1000kV/ms, 0.12kA/ms, and 200kV, respectively [12], [18], and [21]. With an increase of 900% (135Ω) fault resistance, the protection speed of these threshold-based methods declines considerably in the range of few microseconds. However, the selection of lower threshold makes the protection speed faster and vice-versa. Conversely, beyond the safety margin value, the speed of the proposed scheme remains indifferent irrespective of the R_f values. Hence, compared to other methods, the proposed protection method performs better in terms of security and reliability.

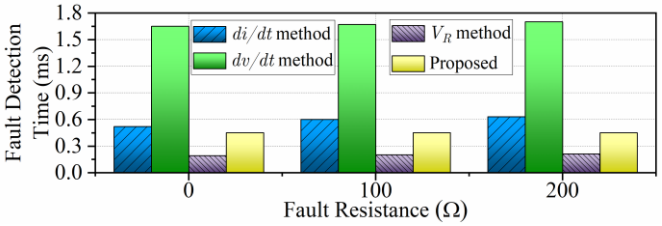

Fig. 15. Comparison of non-unit protection schemes for different fault resistance values.

In response to a line-A PP fault with 10% fault location, the fault detection times of the protection schemes are shown in Fig. 15 for three different R_f values. Considering the respective sampling frequencies (i.e., 20kHz, 20kHz, 5kHz, and 10kHz for *dv/dt*, *di/dt*, V_R, and *V/I* ratio method, respectively), it can be seen in Fig. 15 that the *dv/dt* method is a relatively slow detection method, and, conversely, the V_R method is the quickest to respond. For a large R_f value of 200Ω, the detection of the proposed scheme takes a bit longer of 240μs compared to the V_R method. However, the detection speed of the proposed method can be enhanced significantly by increasing the sampling frequency.

Concerning the selectivity and sensitivity, the proposed scheme performs better compared to other protection schemes. The threshold settings are mandatory for all the protection schemes except the proposed one, and a higher threshold value eventually increases the selectivity with reduced sensitivity. Although all other protection methods mentioned above can sense high fault resistance, they require a relatively longer time (in μs) to respond with increasing values of R_f as revealed in Figs. 14 and 15. Taking the *dv/dt* method as an example, the gradual increase of R_f value (0 to 200Ω) causes an increase of 50μs for the detection time. Consequently, a large R_f value influences the sensitivity of the protection methods. On the contrary, due to the absence of a threshold value, the proposed scheme is not altogether affected by a large R_f as shown in Figs. 14 and 15, thereby, improves the selectivity.

VII. CONCLUSIONS

This paper proposes a novel fault identification technique for DC transmission lines based on the *V/I* ratio of a current limiting reactor. The contributory findings of the proposed method are listed below:

1) With the *V/I* ratios of three sampling intervals, the DC fault is accurately identified without any threshold setting. Simulation results verified in a large MTDC grid reveal that the protection method is highly selective in detecting, discriminating, and locating DC faults from single-ended measurements.

2) The parallel computation of the fault discrimination and location makes the proposed scheme faster to respond. The complete fault event is identified in a time much lower than 1ms with a location accuracy of around 99%.

3) Based on the sensitivity analysis it is evident that the parameter variation of the DC grid fault has less impact on this method.

4) The proposed scheme can perform efficiently with a lower sampling frequency.

5) The transient events apart from DC faults fail to trigger the protection scheme and thus prove to be highly robust.

6) The comparison results exhibit an improved performance of the threshold-free protection scheme.

In a nutshell, the proposed scheme appears to be a highly selective localized scheme for successful DC fault identification.

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