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Comment on "Catastrophic degradation of the interface of epitaxial silicon carbide on silicon at high temperatures" [Appl. Phys. Lett. 109, 011604 (2016)]

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The authors of a recently published letter[1] state the purpose of their work as an evaluation of the stability of SiC/Si hetero-junctions at high temperatures. The central finding is that temperature annealing at 1100 °C leads to "catastrophic degradation" of "the diode behaviour of the initial p-Si/n-SiC junction." The key electrical measurements that underpin these statements were performed on in-house SiC films,[2] grown at 1000 °C on p-type Si substrates. The measurements were performed on bare Si samples and on n-SiC/p-Si samples before and after annealing. It was found that the 1100 °C annealing changes the initially measured n-type conduction, with a sheet resistance of $R_{SiC} = 1354\,\Omega/\square$, to p-type conduction and a very small sheet resistance of $24\,\Omega/\square$. This change from $1354\,\Omega/\square$ (n type) before the annealing to only $24\,\Omega/\square$ (p type) after the annealing is the basis for the central statement of "catastrophic degradation," which is specified as "shorting of the SiC film to the substrate upon annealing with consequent dominance of the carriers in the thick silicon substrate, with relatively high mobility."

In principle, the observed change from n- to p-type conduction could be caused by current leakage into the p-type Si substrate; however, the measured sheet resistance of the p-type Si substrate (R_{Si}) is needed to check this possibility. The authors did not report the measured sheet resistance of the substrate (R_{Si}). Nonetheless, its value can be unambiguously determined from the fundamental relationship[3] that the authors used to calculate the carrier mobility ($\mu_p = 341\,\text{cm}^2/\text{V}\cdot\text{s}$), based on the measured and reported sheet-carrier density ($N_{Si} = 9\times10^{13}\,\text{cm}^{-2}$) and the value of the electron charge (q):

$$R_{Si} = 1/(q\mu_p N_{Si}) = 203\,\Omega/\square.$$

This value is much higher than the measured $24\,\Omega/\square$ of p-type conduction.

Although there is no direct comparison between $203\,\Omega/\square$ and $24\,\Omega/\square$ in the letter, the authors do acknowledge this large discrepancy by comparing the carrier concentrations as the key contributors to the sheet resistances. Specifically, the authors acknowledge that the carrier concentration that is needed to account for the measured $24\,\Omega/\square$ "is an order of magnitude higher than the bulk carrier concentration directly measured on the silicon substrate." Surprisingly, they state that this discrepancy of about an order of magnitude "is plausible as a result of the combined carrier contributions from both silicon substrate and the silicon carbide." The first implication of this key statement is that the contribution of n-type carriers from the silicon carbide should dominate, so that the combined contributions could be about an order of magnitude higher than the contribution of p-type carriers from the silicon substrate alone. If that were the case, the Hall-effect measurements would show n-type conduction, which is inconsistent with the measured p-type conduction. The second implication is that the reported $24\,\Omega/\square$ should be due to parallel conduction through both the n-type SiC film and the p-type Si substrate. If that were the case, the measured sheet resistance would be $1/(1/R_{SiC} + 1/R_{Si}) = 176\,\Omega/\square$, which is much higher from the reported value of $24\,\Omega/\square$. The fact that neither implication is consistent with the reported measurements means that the measured change from $1354\,\Omega/\square$ (n type) before the annealing to only $24\,\Omega/\square$ (p type) after the annealing cannot be due to catastrophic electrical degradation of the n-SiC/p-Si hetero-junction.

To corroborate the junction-degradation hypothesis, the authors reported measurements on as-grown n-type commercial NovaSiC SiC films on p-type Si. The measurements show p-type conduction and the sheet resistance of $180\,\Omega/\square$. Stating that the NovaSiC films were grown at a much higher temperature of 1350 °C, in comparison to the annealing temperature of 1100 °C, the authors conclude that the observed p-type conduction corroborates their hypothesis. The implication of this conclusion is that temperatures above 1100 °C cause "severe electrical shorting of the epitaxial silicon carbide to the underlying substrate," irrespective of the specific properties of the grown SiC film and the specific SiC/Si hetero-junction. This is an overgeneralization that ignores many important differences, such as the difference between 1000 °C and 1350 °C as the growth temperatures, the difference between the alternative-supply and the concurrent supply epitaxies as the growth modes, the difference between the specific carbonization and seed layers, etc. Most importantly, it ignores the fact that $24\,\Omega/\square$ (measured with the annealed in-house films) is very different from both $180\,\Omega/\square$ (measured with the as-grown NovaSiC films) and $176\,\Omega/\square$ (the estimated value based on the hypothesis of hetero-junction leakage). By not ignoring these differences, the presented hypothesis could be considered for the as-grown NovaSiC films, whereas alternative explanations should be

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considered for the very low p-type sheet resistance ($24\,\Omega/\square$) in the case of the annealed in-house films.

Because of these irreconcilable differences between the central hypothesis and the direct electrical measurements for the SiC films annealed at 1100 °C, the presented interpretations of the reported stress data and micrographs are irrelevant.

The concluding paragraph of the letter begins with the following sentence: "The SiC/Si interface instability has crucial consequences on applications where the silicon carbide on silicon is exposed to high temperatures." The high temperature that was used to reach this conclusion is the annealing temperature of 1100 °C. Therefore, this was the selected temperature for the presented evaluation of "the stability of the SiC/Si hetero-junction at high temperatures." However, most high-temperature applications are limited to 600 °C, including various SiC/Si devices used as high-temperature sensors. The implication of the concluding sentence, in the context of the stated purpose of the paper, is that the evaluation at 1100 °C is a kind of Arrhenius-based accelerated evaluation of the stability of the SiC/Si hetero-junction for applications at much lower temperatures. However, the annealing temperature of 1100 °C is higher than the growth temperature of 1000 °C, and no accelerated testing is ever performed at temperatures that are higher than the crystal-growth temperature. The basic principle of accelerated testing is to accelerate the relevant failure mechanisms and not to show that, for example, silicon substrate melts at 1414 °C, which would have happened if the NovaSiC sample was annealed at 100 °C higher temperature than the SiC growth temperature of 1350 °C.

The remaining concluding sentences read as follows: "In particular, this affects not only the use of SiC on silicon for harsh environments, but also the use of SiC on silicon as pseudo-substrate for the growth of III-N and graphene on silicon, as those materials are currently grown at temperatures above 1000 °C. Therefore, we indicate a compelling need to identify a more robust barrier at the SiC/Si interface able to insulate the silicon carbide from the silicon substrate at high temperatures." An implication of this overgeneralized conclusion is that a more robust insulation of the SiC from the Si substrate is needed to enable the use of SiC grown on Si as the pseudo-substrate for the GaN-based blue light-emitting diodes (LEDs). This implication is the exact opposite from the actual requirement to have as small as possible current barrier and resistance to the GaN layer, which acts as the LED cathode.

In conclusion, the central finding that there is a catastrophic electrical degradation of the n-SiC/p-Si hetero-junction is shown to be evidently wrong for the case of SiC films grown on Si by the previously published growth method at 1000 °C.[2] More generally, it is shown that the method of evaluating device applications by annealing at temperatures higher than the crystal-growth temperature is flawed. Therefore, contrary to the authors' final conclusion, there is no "compelling need to identify a more robust barrier at the SiC/Si interface" for possible applications of SiC films grown on Si.

[1] A. Pradeepkumar, N. Mishra, A. R. Kermany, J. J. Boeckl, J. Hellerstedt, M. S. Fuhrer, and F. Iacopi, Appl. Phys. Lett. **109**, 011604 (2016).
[2] L. Wang, S. Dimitrijev, J. Han, A. Iacopi, L. Hold, P. Tanner, and H. B. Harrison, Thin Solid Films **519**, 6443 (2011).
[3] S. Dimitrijev, *Principles of Semiconductor Devices*, 2nd ed. (Oxford University Press, New York, 2012).