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Author

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Growth of Gate Oxides on 4H−SiC by NO at Low Partial Pressures

Daniel Haasmann[1,2,a *], Sima Dimitrijev[1,2,b], Jisheng Han[1,c] and Alan Iacopi[1,d]
[1]Queensland Micro- and Nanotechnology Centre, Griffith University, Brisbane, Queensland 4111, Australia
[2]Griffith School of Engineering, Griffith University, Brisbane, Queensland 4111, Australia
[a]d.haasmann@griffith.edu.au, [b]s.dimitrijev@griffith.edu.au, [c]j.han@griffith.edu.au, [d]a.iacopi @griffith.edu.au

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Abstract. In an attempt to significantly reduce the amount of nitric oxide (NO), commonly used to improve the quality of gate oxides on 4H–SiC, a series of alternative gate oxidation processes using a combination of O_2 and NO gas mixtures at low partial pressures were investigated. The properties of 4H–SiC/SiO_2 interfaces on n-type MOS capacitors were examined by the measurement of accumulation conductances over a range of frequencies. Oxide integrity was evaluated by current–voltage measurements and by the extraction of the conduction band offset barrier heights through Fowler–Nordheim (F–N) analysis. A notable reduction of accumulation conductance, indicating a reduction of near-interface traps (NITs), was observed over all measured frequencies for oxidation processes containing NO with a partial-pressure of only 2%. Gate oxides grown in mixture of O_2 and NO at low-partial-pressures demonstrated a considerable improvement of dielectric properties, increasing the barrier height to near theoretical values.

Introduction

The growth of high quality gate oxides combined with abrupt SiC–SiO_2 interfaces, containing a low density of near-interface traps (NITs), is crucial for the fabrication of reliable metal–oxide–semiconductor field-effect transistors (MOSFETs) with high channel mobility on 4H–SiC. The most significant improvements of interface properties have been reported by direct oxide growth in pure nitric oxide (NO) [1]. Unfortunately the very slow growth rate and toxicity associated with 100% NO has made it impractical for the growth of thick gate oxides required for power SiC MOSFETs. To overcome this issue, it has been shown that thermally grown oxides can be treated with post oxidation anneals in NO to provide acceptable thickness and channel-carrier mobility in 4H–SiC MOSFETs [2, 3]. Post-oxidation anneals in NO have shown a considerable reduction in NIT density [2-5], typically improving the channel mobility by an order of magnitude [3]. Furthermore, it has been shown that these NO anneals also significantly improve Fowler–Nordheim (F–N) electron injection characteristics of 4H–SiC MOS structures by increasing the barrier height between the SiC–SiO_2 conduction bands, which improves the reliability of devices operated at high electric fields and temperatures [6]. The positive effects of NO anneals on gate oxides have been linked to nitrogen found at the SiC–SiO_2 interface through physical studies [1-5, 7]. Among several approaches to further improve the gate oxide process, Cheong *et al*. [8] observed additional positive effects of NO by introducing initial nitridation prior to the oxidation and NO annealing, therefore implementing a *sandwich* (nitridation–oxidation–nitridation) type process using 100% NO nitridation steps. Based on the considerable reduction of SiC–SiO_2 interface roughness, Cheong *et al*. [8] concluded that the initial nitridation process played a key role in avoiding the formation of pronounced *oxide islands* prior to the very beginning of the main oxide growth. Schorner *et al.* [9] reported a promising low field mobility of 48 cm^2/Vs together with a threshold voltage of 0.6 V for lateral enhancement-mode MOSFETs by employing a similar *sandwich* gate oxide growth process. These results combined with the improvements associated with direct oxide growth in NO tend to suggest that the presence of NO throughout the oxidation process may be required to further enhance the properties of SiC/SiO_2 interfaces. However, due to low oxide growth rates, toxicity, and the expense of NO gas, this tends to limit the practicality of developing oxidation processes and

post oxidation anneals in pure NO or mixtures containing high partial pressures of NO to small scale oxidation furnaces due to the sheer volume of gas required. A majority of the nitridation processes in the literature report the use of 100% NO although little is known about the effects of NO nitridation on SiC MOS structures at low partial pressures which may be beneficial for larger oxidation furnaces given the ever increasing size of 4H–SiC wafers.

In this paper, a series of gate oxides grown in mixtures of O_2 and NO at low-partial-pressures to limit the consumption of NO in large furnaces are investigated by evaluating the electrical characteristics of n-type MOS capacitors.

Experimental

All MOS capacitors used in this experimental analysis were fabricated on Si-faced, n-type off-axis 4H–SiC substrates with a 10μm epitaxial layer doped by nitrogen to a concentration of 10^{16} cm^3 by CREE Research . Prior to oxidation, the samples were prepared using a Radio Corporation of America (RCA) cleaning procedure. Gate oxides were thermally grown in an atmospheric furnace at 1250°C by a variation of three different oxidation procedures at low partial pressures. Low partial pressures were achieved by buffering the precursor gasses with inexpensive, inert nitrogen. In light of the significant reduction in growth rate and corresponding improvement in electrical properties of oxides grown in 100% NO, the growth rate of the bulk oxide growth phase, common to all samples, was limited by reducing the partial-pressure of O_2 to 5%. The partial-pressure of NO was restricted to a mere 2% when required, significantly reducing the consumption of the gas. For comparison, three sets of gate oxides were grown. The first oxide was grown in 5% dry O_2 (labelled O_2) for 9 hours as an O_2 only reference sample. A second, *sandwich* type process (labelled NO/O_2/NO) consisted of a 2% NO pre-anneal for 1 hour, followed by the bulk oxide growth in 5% dry O_2, for 9 hours, finalised with a post oxidation anneal in 2% NO for an hour. The final oxidation process was comprised of a 5% dry O_2 and 2% NO (labelled O_2+NO) combined gas mixture for 9 hours. Immediately after oxidation, aluminium gate contacts were sputtered and defined by photolithography to form 500μm squares. Aluminium was also sputtered on the back of the samples to form ohmic contacts.

Interfacial properties of the MOS capacitors were examined by capacitance–voltage (C–V) and conductance–voltage (G–V) measurements. DC voltage was swept between strong-accumulation and deep-depletion values, with a superimposed AC signal amplitude of 50 mV, using a range of frequencies between 1 kHz and 100 kHz at 25°C. The accumulation conductance extracted from the G–V measurements at a constant oxide electric field was analyzed to determine the effect the oxidation processes had on both the density and distribution of NIT's. Oxide integrity was assessed by the extraction of the SiO_2/SiC conduction band offset barrier heights from oxide current density–oxide electric field plots using F–N analysis.

MOS Capacitor Characterization

The high frequency C–V curves of all three oxidation processes at a nominal measurement frequency of 10 kHz are shown in Fig 1. It can be seen that the accumulation capacitance of the oxide processes using NO are significantly higher compared to the standard dry O_2 process. Since all processes share similar bulk oxide growth phase (O_2 for 9 hours), the reduction in oxide thickness indicates that NO substantially retards the oxide growth rate, most likely due to passivation effects. The positive shift of both curves containing NO indicates an increase in net negative charge either due to a reduction of fixed positive oxide charge or an increase of deep electron traps.

In recent work, a method based on the quantum confinement of electrons to quantized two-dimensional subbands in the conduction band and the accumulation conductance of n-type MOS capacitors was proposed to evaluate the existence of NITs aligned to the conduction band [10]. These traps are of particular importance in determining channel mobility as they become electrically active and trap channel electrons through tunneling once the MOSFET is biased into

strong inversion. A detailed example of the measured accumulation conductance at 10 kHz is shown in Fig. 2. Based on the accumulation conductance (V_G > 4V) it can be seen that both processes containing NO show a reduction of the NIT density measured at 10 kHz.

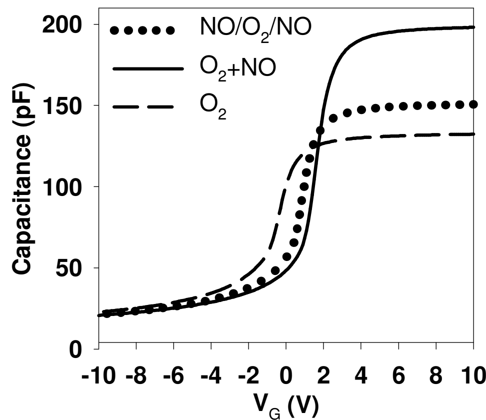

Fig. 1. High frequency C–V measurements of different low-partial-pressure oxidation processes at 10kHz.

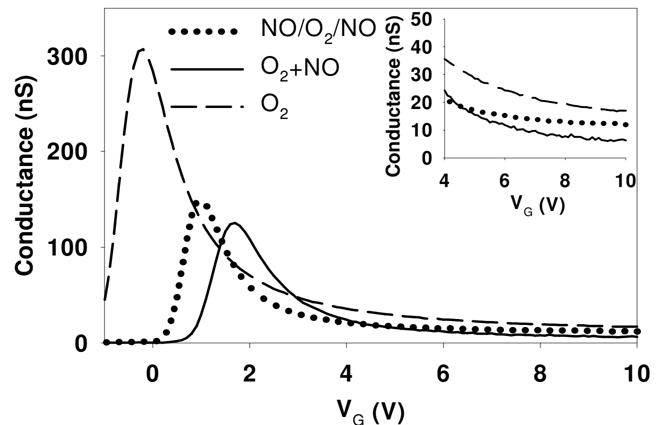

Fig. 2. Comparison of conductance–voltage curves at 10 kHz, indicating active NIT-carrier communication through the measured accumulation conductance.

It was also suggested that accumulation conductance measurements over a range of frequencies can provide information on both the density and distribution of NITs in SiC/SiO_2 MOS structures, where the measurement frequency corresponds to the carrier-NIT tunneling time and therefore carrier-NIT tunneling distance from the SiC/SiO_2 interface. A comparison of the accumulation conductance characteristics over three magnitudes of frequency is shown in Fig. 3. The accumulation conductance was measured at a moderate oxide electric field of 1.5MV/cm to avoid any discrepancies from the variation of oxide thicknesses. All accumulation conductance plots exhibit strong frequency dependence. The higher accumulation conductances at higher frequencies indicate that the NIT density increases closer to the SiC/SiO_2 interface in all oxidation processes. The gate oxides grown with the inclusion of NO show a prominent reduction of NITs throughout the measurement frequency range, demonstrating that the extremely low partial pressure of NO still plays a significant role in improving the properties of the SiC/SiO_2 interface. At higher frequencies, the NO/O_2/NO-*sandwich* process displays the greatest reduction in the density of fast or shallow NITs, most likely due to the NO post oxidation anneal of the interface. It can also be observed that the O_2 reference and O_2+NO combined oxidation processes reveal an exponential increase in NIT density from 10 kHz.

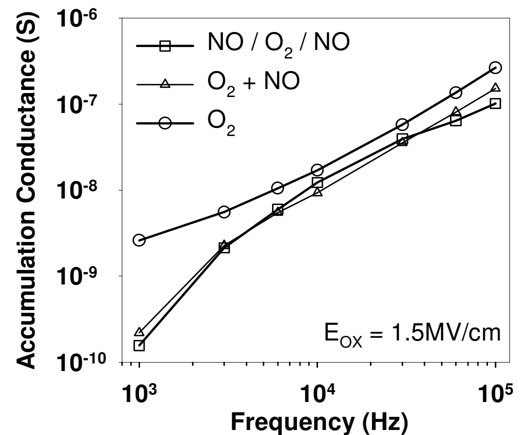

Fig. 3. Semi-lograthmic accumlation conductance–frequency plots of 4H–SiC n-type MOS capacitors measured at a nominal oxide field of 1.5MV/cm.

Current–voltage measurements were performed under positive gate bias at room temperature in order to compare gate oxide conduction characteristics. A typical semi-logarithmic plot of oxide leakage-current density versus oxide electric field is shown in Fig. 4(a). The electric field was calculated by dividing the applied gate voltage, minus the metal-semiconductor work function difference, by the oxide thickness. It can be seen that the electric field, where the F–N conduction mechanism begins to dominate, is significantly higher for the oxide processes incorporating NO. To determine the barrier height between the 4H–SiC/SiO_2 conduction bands, an F–N analysis was performed using the high-field regions of I–V plots where the F–N tunneling was identified as the dominating conduction mechanism. The effective electron mass in the oxide of $0.42m_0$ [6] was used

to calculate the barrier height from the slope of the F–N plots shown in Fig. 4(b). The effective barrier heights were estimated to be 2.33eV, 2.50eV, and 1.95eV for the NO/O_2/NO sandwich, O_2+NO combined, and O_2 oxide processes, respectively. Both NO treated samples exhibited an increase in the barrier height over the O_2 reference process. The combined O_2+NO sample showed the greatest improvement in dielectric properties, exhibiting a barrier height of only 0.2eV lower than the theoretical ideal value of 2.7eV.

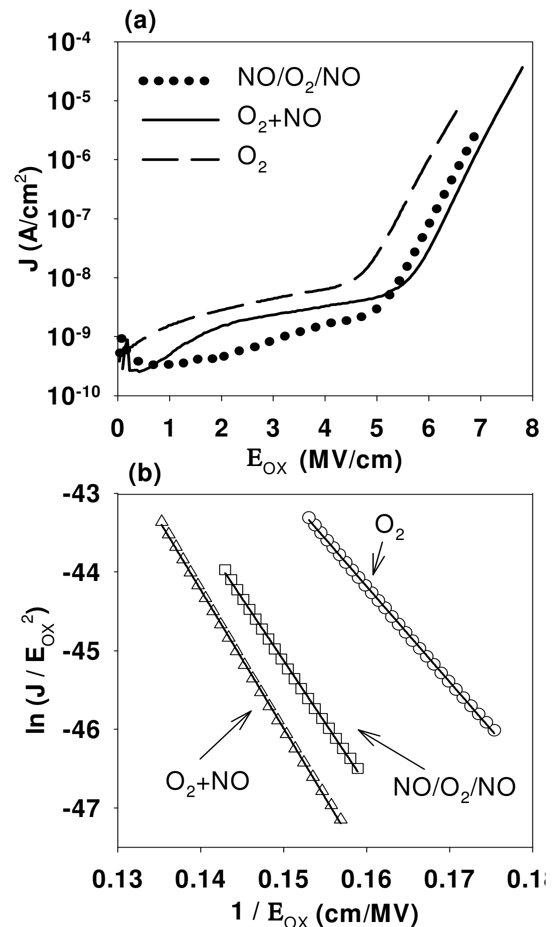

Fig. 4. A typical plot of the oxide leakage current density as a function of applied electric field (a) and the F–N electron injection plots (b) obtained from the *J–E$_{OX}$* measurements of (a).

Summary

Accumulation conductance-frequency and F–N analysis of oxide leakage currents on n-type 4H–SiC MOS capacitors with oxidation processes containing O_2 and NO at low partial pressures were investigated. Significant improvements of the SiO_2 interface and oxide integrity were still observed with oxidation processes employing an extremely low 2% partial pressure of NO, compared to that of dry O_2 only. The samples oxidized in an NO/O_2/NO *sandwich* type process exhibited the greatest reduction of NITs closer to the SiC/SiO_2 interface, whereas samples oxidized in a combined O_2+NO process demonstrated a considerable enhancement in oxide integrity, exhibiting barrier height of only 0.2eV less than the theoretical value of 2.7eV. The barrier height was increased 0.55eV over the sample oxidized in an O_2 only ambient. These promising results highlight the significance of NO even at extremely low partial pressures. The alternative oxidation processes, investigated in this study, substantially reduce the amount of NO required, which is a favorable consideration for 4H–SiC gate oxidations in large scale furnaces, while improving the electrical quality of the SiC/SiO_2 interface.

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