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Full Wave Solution for Intel CPU with a Heat Sink for EMC Investigations

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***Abstract* — A CPU with a heat sink (e.g. Intel Pentium 4 and Intel Pentium dual core) is one of the challenging problems for IEEE EMC. A Very Large Scale Integrated (VLSI) device was modelled using the Finite Element Method (FEM) frequency domain as this provides a 3D full wave solution. The electromagnetic (EM) radiation emitted from these high power microelectronic circuits connected to a heat sink was found to have resonant frequencies around 2.4 GHz and 5 GHz with a reflection coefficient less than 19 dBi and 8 dBi. Those resonant frequencies are very close to the operating frequency of both IEEE and Bluetooth wireless communication systems. This paper proposes a new benchmark model based on a dual core CPU.**

I. INTRODUCTION

Modern silicon wafer fabrication facilities easily produce component densities that exceed 1 million transistors per die. The power generated from processor currents can exceed 100W with increasing high clock speeds. This combination of switching frequency and power level, in conjunction with the layout of the common mode current paths through the heat sinks, results in a significant level of radiated Electromagnetic Interference (EMI). As a result, circuit designers require an understanding of the radiated emissions from the CPU and its heat sinks. Designers also need to find ways to reduce these emissions. Components such as the Intel Pentium 4, Intel Pentium dual core CPU, and AMD Athlon dual core CPU require separate cooling procedures provided by a fan built into their heat sink or by a fan or cooling device located adjacent to the processor. Since these high-power and high-speed processors are common in recent designs, special techniques are required for EMI suppression and heat removal at the component level. In addition, 3D EM full wave based numerical analysis tools are required to model the radiated emissions. This paper focuses mainly on RF radiated emission problems that consider the EMC source modelling for the CPU and heat sink as a RF radiator [1].

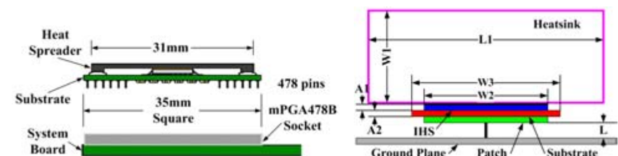
II. EMC SOURCE MODELLING AND MODEL ATTRIBUTES

A. CPU Source Model Consideration

EMC/EMI models are commonly represented as three distinct parts: the source of RF energy, the geometry of the model components, and the remaining problem space [2]. To model the CPU with a heat sink structure, it is useful to further divide the structure into three regions; the ground plane, source region and heat sink. A realistic representation of a VLSI circuit must consider the electromagnetic source characteristics and an actual physical representation such as a conducting patch [3]. Although real heat sinks have fins to increase the thermal convection loss, Brench [4] found that the heat sink could be modelled as a solid block. Das and Roy [5] modelled the source as a monopole that passes through the circuit. This EMC source model was used to address the previous problem confronting the IEEE EMC (486 CPU). The Intel P4 and Intel dual core CPU with a heat sink have completely different structural configurations, therefore a new EMC source model is required for modelling and simulation.

B. Intel P4 CPU Heat Sink and Source Model

The Intel P4 processor with the 478-Pin has different packaging and a different structural configuration (see Figure 1a). In the Intel P4 configuration, a heat spreader is located on top of the VLSI. This heat spreader is electrically isolated from the VLSI packaging. A new EMC source model consists of a multi layered structure forming a microstrip patch antenna structure, which is resonant at frequencies of around 2.4 GHz and 5 GHz respectively. This is shown in Figure 1(b). Several clock frequencies in the band from 1.40 GHz through 2GHz are considered for demonstration purposes, where A1 is 2.378mm, A2 is 1.080mm, L is 2.030mm, L1 is 88.9mm, W1 is 38.1mm, W2 is 31.75mm and W3 is 35mm.

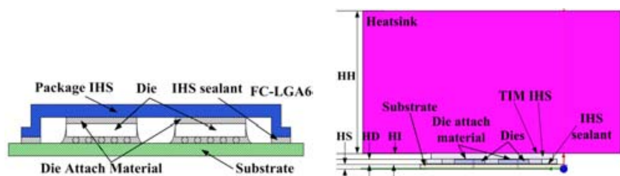


(a) Intel P4 CPU and packaging (b) EMC source model with a heat sink
Figure 1. Intel P4 CPU heat sink configuration and simulation model.

C. Intel Dual Core CPU Heat Sink Model

A transverse cross-section of the Intel dual die processor with a heat sink is illustrated in Figure 2. The package is a Flip-Chip Land Grid Array (FC-LGA6) and the die is located upon the substrate with the help of die attach material. The sealing is also the integrated heat spreader (IHS) covering the dies in order to protect them. Adhered by the thermal interface material (TIM), the heat sink is in full contact with the top of IHS. Like the Intel P4 CPU model, this dual core CPU model can be simplified to a dual feed microstrip patch antenna structure. The location of feed points is a critical factor that affects the accuracy and validation of the simulation results. Based on the heat distribution on an existing Intel dual die CPU [7], the hottest point is predicted to be the area of highest current distribution where the electromagnetic interference

generated is very significant. Thus the feed points of the equivalent patch were allocated to these regions for the EMC source model assuming a 50 ohm source. Note that the highest current density for a driven patch antenna is immediately adjacent to these probe feeds. The size of the equivalent patch antenna model is simply the resonant size at 2.45 GHZ and the second frequency at 5 GHz.



(a) Intel Dual Die packaging (b) EMC source model with a heat sink

Figure 2. Intel dual core CPU heat sink configuration and EMC source model.

III. FULL WAVE SOLUTION

A. Frequency Domain Modelling in EMC/EMI

The most accurate modelling of EMC requires a 3D full-wave solution in which Maxwell's equations are solved. With numerous fast numerical algorithms now available, the FEM in the frequency domain is relatively efficient. The technique finds approximate solutions of partial differential equations and integral equations. The frequency domain vector wave equation for the ***E*** field is:

$$\nabla \times \frac{1}{\mu} \nabla \times \mathbf{E} + \sigma_e \omega \mathbf{E} + \omega^2 \varepsilon \mathbf{E} = -j\omega \mathbf{J} \quad (1)$$

where ω is angular frequency, **J** is the source current, σ_e is the effective conductivity, and μ and ε are the permeability and permittivity of the problem space respectively.

B. Full Wave Solutions for CPU Heat Sink Models

The computation model for the Intel P4 and Intel dual core CPU heat sink fits within the source models developed in this work. These are shown in Figures 1 and 2, where the absorbing boundary condition, PML, is used to surround the computation model to obtain accurate results. The excitation is a vertical probe extending from the ground plane to the base of the conducting patch.

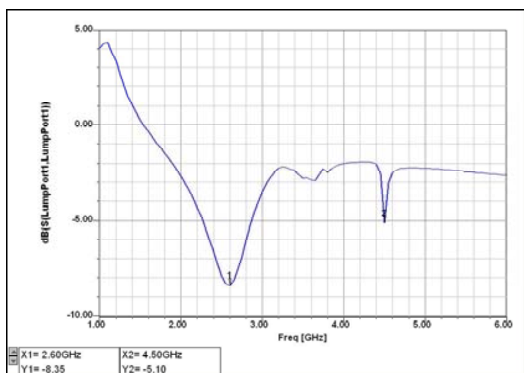


Figure 3. S_{11} impedance matching for the Intel P4 CPU heat sink model.

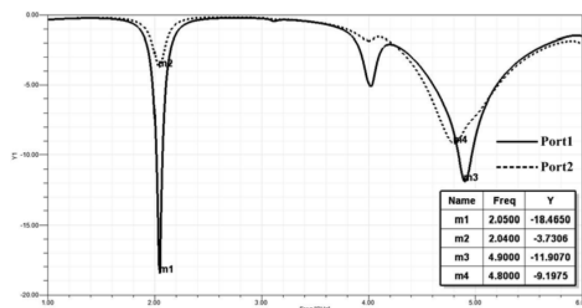


Figure 4. S_{11} impedance matching for the Intel dual core CPU heat sink, where — line indicates the excitation at port 1, and … line indicates the excitation at port 2. The mark position is indicated by m1, m2, m3 and m4.

This is electromagnetically coupled to the heat sink through the substrate. Figures 3 and 4 show the scattering parameter S_{11} (with a 50 ohm source) across the frequency band. Both models have two resonant frequencies. The S_{11} results indicate that there is maximum radiation from the structure at these two frequencies. The CPU heat sinks cause significant radiated emissions at these frequencies, assuming it is possible that currents in the VLSI circuit have Fourier components at these frequencies.

IV. CONCLUSION

This paper presents a FEM based computation technique for radiated emissions from CPU heat sink models. The CPU heat sink model is significantly different to the conventional CPU heat sink model of IEEE EMC challenge problems. The Intel P4 and Intel dual core CPU heat sink models with insulated configurations were found to radiate at 2.4 GHz and 5 GHz respectively. These two frequencies lie very close to the wireless communication range in computing systems. The source model selection is critical for the CPU heat sink model as it affects the resonant frequencies associated with the CPU clock speed, the CPU core and heat sink structures. The far field radiation patterns from those CPU heat sink models and validation of the CPU dual core benchmark model will be discussed in the full paper.

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