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The Fundamental Current Mechanisms in SiC Schottky Barrier Diodes: Physical Model, Experimental Verification and Implications

S. Dimitrijević, J. Nicholls, P. Tanner, and J. Han

Abstract – In this paper, we derive the equations for the current–voltage characteristics of SiC Schottky barrier diodes from the fundamental physics of thermionic emission and tunneling, as the two fundamental current mechanisms. An excellent fit between the model and the experimental data is achieved without the need for empirical fitting parameters, such as the commonly used ideality factor, and with a single set of physically meaningful parameters. This result shows that the current transport in the measured SiC Schottky diodes is not dominated by defects.

I. INTRODUCTION

Metal–semiconductor contacts and the energy barriers that they form exist in all semiconductor devices. Two fundamental current mechanisms that enable current to flow through metal–semiconductor contacts are (1) thermionic emission of carriers over the contact barrier and (2) carrier tunneling through the barrier. In spite of the fact that metal–semiconductor contacts are so common, there is a significant degree of confusion regarding the models and the parameters of the two fundamental current mechanisms [1–6]. A reason for this confusion has been the absence of experimental results that could be modeled without the need to include second-order effects. For example, carrier generation and recombination impact the carrier transport through contacts made on silicon substrates [7,8].

Silicon carbide is a wide energy-gap material, which does not suffer from carrier generation and, in the case of metal contacts to N-type SiC, there is no recombination because there are no holes in this semiconductor. Accordingly, this material provides an excellent platform for an experimental-based verification of the fundamental current mechanisms. The adequate structure for this purpose is a Schottky-barrier diode with proper edge terminations, to ensure that the measured current is through the planar region of the contact. This structure is shown in Fig. 1a.

Commercial SiC Schottky diodes have been available for more than a decade. However, the structure of these

diodes is different (Fig. 1b)—it is known as Junction Barrier Schottky (JBS) diode because it utilizes P+/P pockets to protect the semiconductor surface from the highest electric field by a dense array of reverse-biased P–N junctions. Consequently, the reverse-bias current of these diodes is dominated by the complex two-dimensional structure of the reverse-biased P–N junctions.

Recently, we have fabricated pure SiC Schottky diodes with an adequate edge termination (Fig. 1a), which are suitable for the experimental verification of the fundamental current mechanisms that we discuss in this paper. It should be mentioned that pure SiC Schottky diodes are now also available from Rohm (a large power-device manufacturer from Japan).

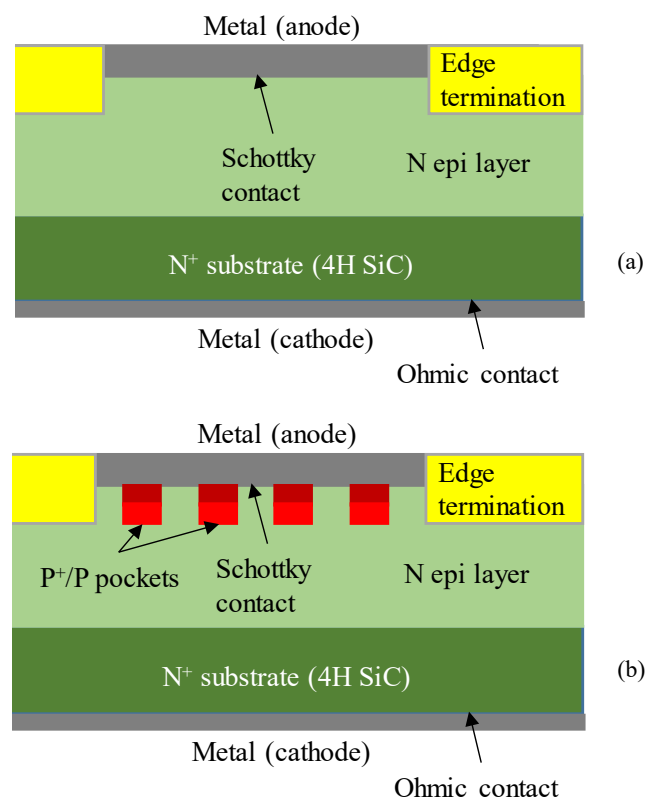


Fig. 1. Cross-sectional diagrams of a pure Schottky diode used in this paper (a) and the most commonly available junction-barrier Schottky (JBS) diode (b).

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II. ENERGY BANDS

The energy-band diagram of a typical metal–SiC contact with aligned Fermi levels (E_F) is shown in Fig. 2. We consider the electrons in both metals and in the conduction band of a semiconductor as free carriers with the effective mass m^* (in addition to the generic symbol m^* , we will also use the notations m_m^* and m_s^* to distinguish between the values of the effective mass in the metal and in the semiconductor, respectively). According to the free-carrier model, the kinetic energy of electrons is $E_{kin} = m^*v_{th}^2/2$, where v_{th} is the thermal velocity of electrons. The condition $E_{kin} = 0$ corresponds to the bottom of the conduction band in the semiconductor (E_C), which is above the Fermi level, and to the bottom of the band in the metal, which is well below the Fermi level. In the case of aluminum, illustrated in Fig. 2, E_F is 5.6 eV above the bottom of the band, which corresponds to $v_{th} = 1.4 \times 10^6$ m/s for $m^* = m_0 = 9.1 \times 10^{-31}$ kg and for the electrons with $E_{kin} = E_F$ (note that this is 4.7% of the speed of light).

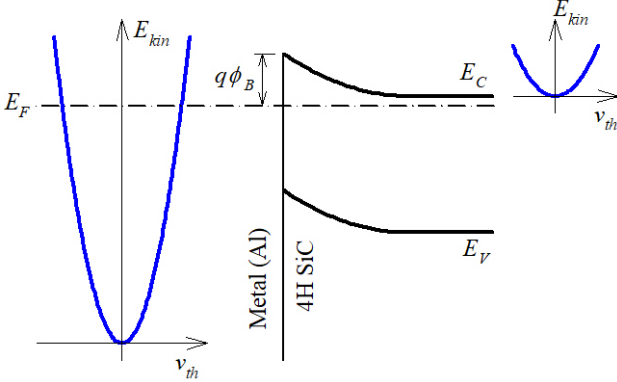


Fig. 2. Energy-band diagram of a typical metal–SiC Schottky contact with aligned Fermi levels (E_F) and with illustrations of the kinetic energies ($E_{kin} = m^*v_{th}^2/2$) of electrons in the metal and in the semiconductor. E_C and E_V are the bottom of the conduction band and the top of the valence band in SiC, respectively.

The most important parameter of a Schottky contact is the energy-barrier height, labeled by $q\phi_B$ in Fig. 2. The fundamental factor contributing to the formation of the barrier is the difference between the work function of metal and the electron affinity in the semiconductor [9]. For example, the difference between the work function of aluminum ($q\phi_m = 4.25$ eV [10]) and the electron affinity of 4H SiC ($q\chi_s = 3.6$ eV [11]) is 0.65 eV. However, this value is well below the experimentally observed barrier heights.

In real metal–semiconductor contacts, the existence of trapped charge (Q_{nit}) at distance δ from the metal surface creates an electric field, Q_{nit}/ϵ_s , which causes bending of the energy bands by the factor $q\delta Q_{nit}/\epsilon_s$ [12]. The traps that are responsible for this additional component of the

barrier height are usually referred to as interface traps [12]; however, we have suggested recently the use of the term “near interface traps”, to highlight the fact that the charge associated with pure interface traps ($\delta = 0$) is fully compensated by the charge in the metal and, hence, does not create electric field and does not contribute to the band bending [13].

The third factor that impacts the barrier height is the image-force effect, which reduces the barrier by $q\Delta\phi_B = 2q\sqrt{qE_S/16\pi\epsilon_s}$, where E_S is the electric field at the surface of the semiconductor and ϵ_s is the semiconductor permittivity [12].

The following equation summarizes the described contributions to the barrier height at a metal–semiconductor contact with aligned Fermi levels:

$$q\phi_B = q\phi_m - q\chi_s + \frac{q\delta Q_{nit}}{\epsilon_s} - 2q\sqrt{\frac{qE_S}{16\pi\epsilon_s}} = q\phi_{B0} - 2q\sqrt{\frac{qE_S}{16\pi\epsilon_s}} \quad (1)$$

In Eq. (1), $q\phi_{B0}$ is a single material parameter, incorporating the difference between the metal work function and the electron affinity of SiC, as well as the contribution of the charge at near-interface traps when the Fermi level of the semiconductor is aligned to the Fermi level of the metal.

III. METAL-TO-SEMICONDUCTOR CURRENT

In their thermal motion inside the metal, a number of electrons hit the interface with semiconductor. If we set the x direction to be normal to the interface and label the thermal velocity in the x direction by v_{th-x} , the number of hits per unit area and unit time is

$$N_{hits} = v_{th-x}n \quad (2)$$

where n is the concentration of electrons. Most of these electrons will bounce back, but some of them pass through the interface, either by tunneling or thermionic emission (Fig. 3). If we label the probability that an electron will traverse the interface by P and the electron charge by q , we obtain the following basic equation for the current density of electrons flowing from the metal into the semiconductor:

$$j_{m \rightarrow s} = qPN_{hits} \quad (3)$$

In Eq. (3), both the probability P and the number of hits are variables that depend on the kinetic energy $E_{kin-x} = m^*v_{th-x}^2/2$. To account for this effect, we rewrite Eq. (3) in the following form

$$j_{m \rightarrow s} = \int_0^\infty qP(E_{kin-x})n_{hits}(E_{kin-x})dE_{kin-x} \quad (4)$$

where $n_{hits}(E_{kin-x})$ is the number of hits per unit area, unit time, and unit energy. Taking into account the density-of-states distribution with energy, the Fermi–Dirac distribution for the probability of state occupancy, and assuming that electrons move randomly in all directions, we have derived the following equation for $n_{hits}(E_{kin-x})$ in a recently published paper [14]:

$$n_{hits}(E_{kin-x}) = \frac{4\pi m^* kT}{h^3} \ln \left[1 + \exp \left(\frac{E_F - E_{kin-x}}{kT} \right) \right] \quad (5)$$

where T is the absolute temperature, k is the Boltzmann constant, and h is the Planck constant.

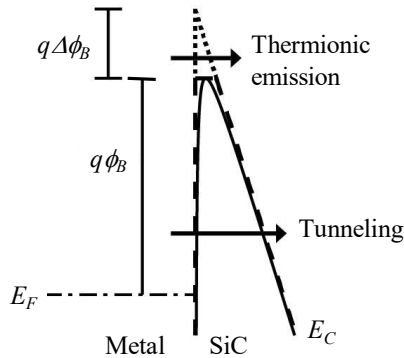


Fig. 3. Illustration of thermionic emission and tunneling as the two mechanisms of electron flow from metal to semiconductor, which dominate the reverse-bias current of Schottky diodes ($q\phi_B$ is the barrier height and $q\Delta\phi_B$ is the barrier reduction due to the image-force effect).

In Eq. (4), $P(E_{kin-x}) = 1$ for the case of thermionic emission, when $E_{kin-x} > E_F + q\phi_B$. Regarding the tunneling mechanism, we used the Wentzel–Kramers–Brillouin approximation to derive the following equation for $E_{kin-x} < E_F + q\phi_B$ [14]:

$$P(E_{kin}) = \exp \left[-\frac{4\pi\sqrt{2m_t^*}}{h q E_S} \sqrt{E_\phi} \left(\frac{2}{3} E_\phi + q\Delta\phi_B \right) \right] \quad (6)$$

where m_t^* is the tunneling effective mass, E_S is the electric field at the surface of the semiconductor, $E_\phi = E_F + q\phi_B - E_{kin-x}$, and $q\Delta\phi_B = 2q\sqrt{qE_S/16\pi\epsilon_S}$.

To verify the model represented by Eqs. (4)–(6), we measured reverse-bias currents at different temperatures and for diodes designed for blocking voltages of 650 V and 1200 V. The results for a typical 650-V diode are shown in Fig. 4. We can see that the model fits the data well at higher temperatures, whereas the experimental current is higher at room temperature. We also observed that there is a device-to-device variation of measured currents at room temperature, which does not exist when the measurements are performed at higher temperatures. This indicates that the

measured room-temperature currents include significant leakage components through defects, which become insignificant at higher temperatures.

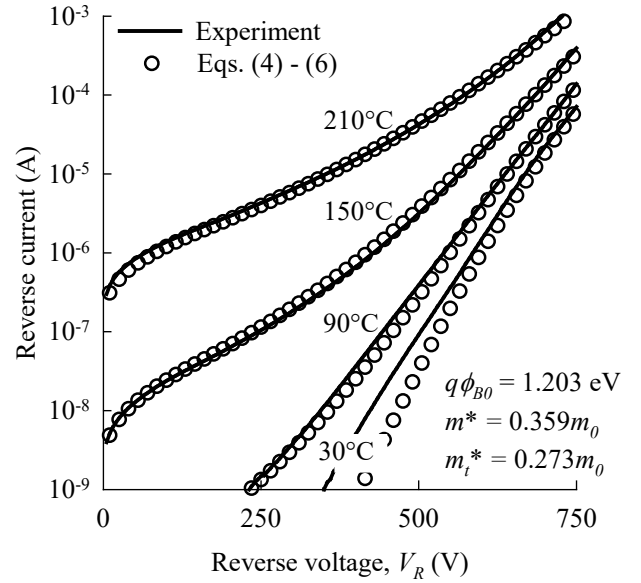


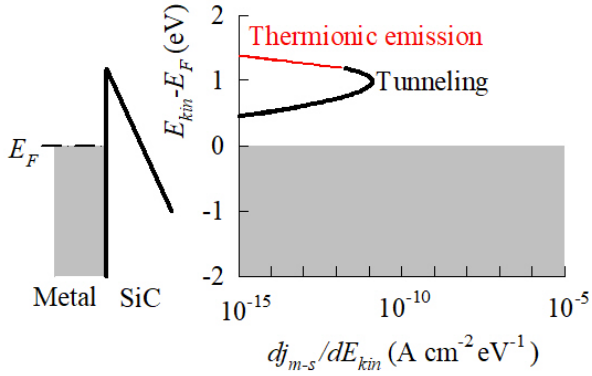
Fig. 4. Verification of the model for metal-to-semiconductor current by measured reverse-bias currents at different temperatures. Note that $q\phi_{B0} = q\phi_B + q\Delta\phi_B$.

In semiconductor theory, we frequently approximate the population of electron states by stating that the energy levels below the Fermi level are occupied, whereas those above the Fermi level are empty. With this assumption, and with reference to Figs. 2 and 3, it appears that the metal-to-semiconductor current would be dominated by tunneling of electrons with energies around the Fermi level. Given that tunneling is a temperature-independent mechanism, it is surprising to see in Fig. 4 the large temperature dependence of the reverse-bias current.

The surprise is due to the wrong assumption that the metal-to-semiconductor current is dominated by electron with energies around E_F . It is correct that the concentration of electrons well above E_F drops exponentially, but the tunneling probability increases exponentially for electrons with E_{kin-x} well above E_F . In Fig. 5, we show calculations of the function inside the integral of Eq. (4) for two different reverse-bias voltages, $V_R = 150$ V and 650 V, corresponding to the electric fields at the semiconductor surface of $E_S = 6.6 \times 10^5$ V/cm and 1.5×10^6 V/cm, respectively. We can see that the peak of the current for $V_R = 150$ V is just below the tip of the barrier, which is about 1 eV above the Fermi level. With this insight, it becomes obvious that an increase in the temperature can cause a significant current increase by increasing the concentration of electrons around the tip of the energy barrier. Figure 5b shows that the peak of the current drops toward the Fermi level at $V_R = 650$ V. This again shows that a small fraction of the metal electrons contribute to the reverse-bias current

and that the current increases when the temperature increases the concentration of these electrons.

(a) $V_R=150$ V ($E_S = 6.6 \times 10^5$ V/cm)



(b) $V_R=650$ V ($E_S = 1.5 \times 10^6$ V/cm)

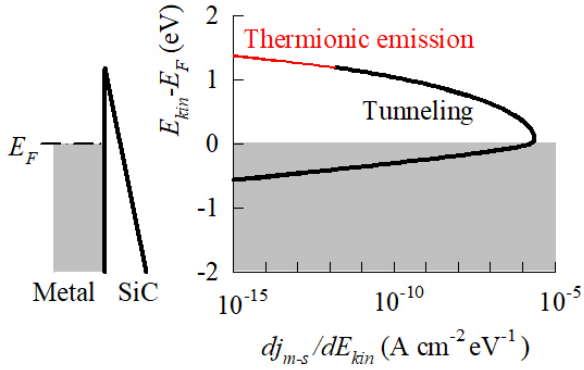


Fig. 5. Distributions of metal-to-semiconductor current at two different reverse-bias voltages: (a) 150 V and (b) 650 V.

IV. SEMICONDUCTOR-TO-METAL CURRENT

The flow of electrons from the semiconductor to metal is responsible for the forward-bias current. Figure 6 illustrates the energy bands at forward bias and shows that the dominant mechanism is thermionic emission of conduction-band electrons over the barrier (in this case, tunneling through the barrier is insignificant in comparison to the thermionic current). The kinetic energy of the electrons hitting the semiconductor–metal interface is $E_{kin-x} > 0$, which means their total energy is larger than E_C and, consequently, the probability that they will pass through the interface is $P(E_{kin-x}) = 1$. With this, the general equation for the current density of electrons flowing from the semiconductor into the metal is

$$j_{s \rightarrow m} = \int_0^{\infty} q n_{hits}(E_{kin-x}) dE_{kin-x} \quad (7)$$

The derivation of the equation for the number of hits per unit area, unit time, and unit energy, $n_{hits}(E_{kin-x})$, is

similar to the derivation of Eq. (5) for the electrons in metal with one important difference: As Fig. 2 shows, the bottom of the conduction band in the semiconductor is at the energy level E_C above the bottom of the band in the metal. This means that the zero level for both the thermal velocity and the density of states, which corresponds to $E_{kin-x} = 0$, is at E_C in the case of semiconductor. Accordingly, the energy term in the Fermi–Dirac distribution is no longer just $E_{kin-x} - E_F$ but $E_{kin-x} + E_C - (E_F + qV)$, where $E_F + qV$ is the quasi-Fermi level in the semiconductor. With that, the logarithm term in Eq. (5) becomes $\ln \left[1 + \exp \left(-\frac{E_{kin-x} + E_C - E_F - qV}{kT} \right) \right]$, which can be approximated by $\exp \left(-\frac{E_{kin-x} + E_C - E_F - qV}{kT} \right)$ given that $E_{kin-x} + E_C - E_F - qV \gg kT$. Therefore, the equation for the number of hits per unit area, unit time, and unit energy becomes

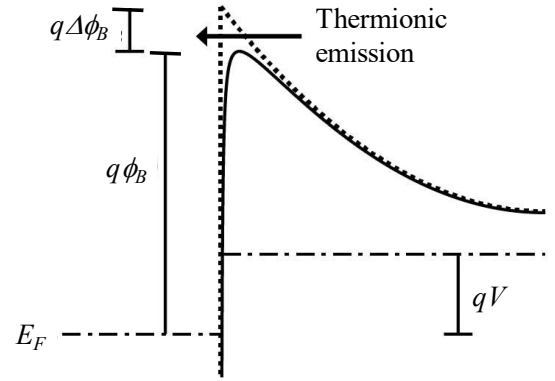


Fig. 6 Illustration of thermionic emission as the mechanism of electron flow from semiconductor to metal, which is responsible for the forward-bias current of Schottky diodes. Note that $q\phi_B = q\phi_{B0} - q\Delta\phi_B + \frac{q^2\delta D_s}{\epsilon_s} V$ where $q\phi_{B0}$ is the barrier height without the image-force effect at $qV = 0$ (a voltage-independent parameter), qVD_s is the number of near-interface traps per unit area in the energy range between the quasi-Fermi levels, and δ is the distance of the near-interface traps from the metal surface [14].

$$n_{hits}(E_{kin-x}) = \frac{4\pi m^* kT}{h^3} \exp \left(-\frac{E_{kin-x} + E_C - E_F - qV}{kT} \right) \quad (8)$$

With this equation for $n_{hits}(E_{kin-x})$, the integral in Eq. (7) can be solved, leading to the following result for the current density of electrons flowing from the semiconductor into the metal:

$$j_{s \rightarrow m} = A^* T^2 \exp \left(-\frac{q\phi_B}{kT} \right) \exp \left(\frac{qV}{kT} \right) \quad (9)$$

where $q\phi_B = E_C - E_F$ and $A^* = \frac{4\pi q m^* k^2}{h^3}$ is the so-called Richardson constant.

According to Eq. (9), the slope of the semi-logarithmic plot, $\ln j_{s \rightarrow m}$ versus V , is equal to q/kT . However, the slope

of measured forward-bias currents is always somewhat smaller than this theoretical value. It is a common practice to reduce the theoretical slope by a fitting parameter called the ideality factor, n , so that the slope becomes q/nkT . This discrepancy between the experimental data and the theoretical slope of q/kT is attributed to several different phenomena [3, 15–17].

The need to introduce the ideality factor is due to the inherent assumption that the barrier height $q\phi_B$ does not change with applied voltage (if we ignore the small impact through a small reduction of the electric field E_S). Referring to Eq. (1), we can see that the assumption of constant $q\phi_B$ corresponds to the implicit assumption of constant charge at the near-interface traps, Q_{nit} . The assumption that the charge at the near-interface traps does not increase as the quasi-Fermi level in the semiconductor is lifted by the applied voltage (qV in Fig. 6) is equivalent to the assumption that there are no near-interface traps with energy levels above the Fermi level of metal. However, if the density of these traps per unit area and unit energy is not zero ($D_{nit} > 0$), they will increase the barrier height as they trap additional electrons when the quasi-Fermi level is lifted by the applied voltage:

$$q\phi_B = q\phi_{B0} - 2q\sqrt{\frac{qE_S}{16\pi\epsilon_s}} + \frac{q^2\delta D_{nit}}{\epsilon_s}V \quad (10)$$

Note that, in Eq. (10), qVD_{nit} is the charge per unit area trapped at the near-interface traps with energy levels between the quasi-Fermi level in the semiconductor and the Fermi level in metal (E_F). Regarding the charge at the near-interface traps with energy levels below E_F (the charge Q_{nit}), Eq. (1) shows that it is included in the term $q\phi_{B0}$.

Figure 7 shows that the fundamental equation for the thermionic emission of electrons [Eq. (9)] is an adequate model for the forward-bias current when the increase in the barrier height due to additional electron trapping [eq. (10)] is included. This means there is no need for the inclusion of the ideality factor as an empirical fitting parameter, which does not provide a direct relationship to a physical mechanism.

The experimental results in Fig. 7 show that the semi-logarithmic plots of measured currents are linear up to currents of about 100 mA. For the higher current levels, the forward voltages are higher than the values corresponding to Eqs. (9) and (10). This is the effect of serious resistance of the drift region and the substrate (r_S), which is simply accounted for by the Ohm's law:

$$V_F = V + r_S I_F \quad (11)$$

where V_F is the measured forward voltage and I_F is the measured forward current.

V. THERMAL EQUILIBRIUM

With verified equations for the current density from metal to semiconductor (Section III) and the current density

from semiconductor to metal (Section IV), it is interesting to consider the condition for thermal equilibrium, which is $I_F = 0$ for $V_F = 0$.

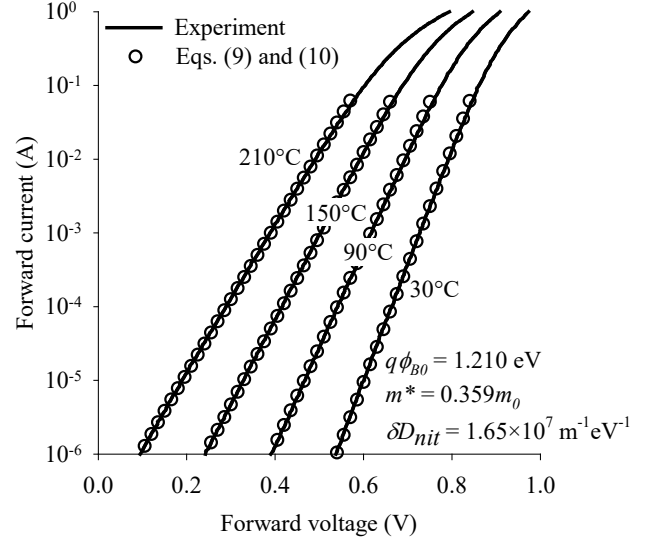


Fig. 7 Verification of the model for semiconductor-to-metal current by measured forward-bias currents at different temperatures.

Neglecting the electron tunneling from metal into semiconductor at zero bias, and approximating the logarithm term in Eq. (5) by $\exp\left(-\frac{E_{kin-x}-E_F}{kT}\right)$, Eqs. (4)–(6) can be written in the following simplified form:

$$j_{m \rightarrow s} = \frac{4\pi q m_m^* kT}{h^3} \int_{E_F + q\phi_B}^{\infty} \exp\left(-\frac{E_{kin-x}-E_F}{kT}\right) dE_{kin-x} \quad (12)$$

Note that we labeled the effective mass by m_m^* to specify that this is the mass of electrons in the metal. Solving the integral in Eq. (12), we obtain

$$j_{m \rightarrow s} = \frac{4\pi q m_m^* kT}{h^3} \exp\left(-\frac{q\phi_B}{kT}\right) \quad (13)$$

The semiconductor-to-metal current at zero bias, obtained from Eq. (9), is

$$j_{s \rightarrow m} = \frac{4\pi q m_s^* kT}{h^3} \exp\left(-\frac{q\phi_B}{kT}\right) \quad (14)$$

In this case, we label the effective mass by m_s^* to specify that this is the mass of electrons in the semiconductor.

The currents $j_{m \rightarrow s}$ and $j_{s \rightarrow m}$, given by Eqs. (13) and (14), respectively, would be equal and the net current at zero bias would be zero if $m_m^* = m_s^*$. However, there is no reason for this condition to be valid in different materials, such as the metal and the semiconductor in the case of Schottky diodes. To explain the consequence of this difference, assume that $m_m^* > m_s^*$. What happens then is that the excess flow of electrons from the metal into the

semiconductor, when $j_{m \rightarrow s} > j_{s \rightarrow m}$, is lifting the bands to reduce the barrier height for the thermionic emission of electrons from the semiconductor and to reach the condition $j_{m \rightarrow s} = j_{s \rightarrow m}$. This band bending is equivalent to the following shift in the semiconductor quasi-Fermi level with respect to E_F [14]:

$$qV_m = kT \ln \left(\frac{m_m^*}{m_s^*} \right) \quad (15)$$

Reducing the barrier height in Eq. (14) by this value leads to the following equation for the semiconductor-to-metal current:

$$j_{s \rightarrow m} = \frac{4\pi q m_m^* kT}{h^3} \exp \left(-\frac{q\phi_B}{kT} \right) \quad (16)$$

This result shows that, effectively, the current from the semiconductor into metal is determined by the effective mass of electrons in the metal, in agreement with experimental results showing that the effective mass is affected by the choice of metal [14,18,19].

VI. CONCLUSION

The reverse-bias current through the metal–semiconductor contact of pure SiC Schottky diodes with an adequate edge termination is dominated by thermionic emission at lower reverse-bias voltages and by tunneling at higher voltages. An excellent fit with experimental data is achieved by a model based on the probability that an electron with a given kinetic energy will pass through the contact—either by tunneling or thermionic emission—and by a determination of the number of hits per unit area, unit time, and unit energy. An analogous model for the thermionic current of a forward-biased diode provides an excellent fit with measured forward-bias currents at different temperatures. This fit is achieved by including a barrier-increase effect due to trapping of electrons by near-interface traps with energy levels between the quasi-Fermi level in the semiconductor and the Fermi level in the metal. By including this physical mechanism, there is no need for the commonly-used empirical fitting parameter known as the ideality factor.

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