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Abstract

The design, development and application of an automated electrical cable harness testing system (ECHTS) with the capability of testing diverse cable harness configurations is presented. The ECHTS is able to test up to 32 conductors via an interchangeable connector, expandable to an additional 32 conductors through the use of an expansion board, detecting open- and short- circuit and incorrect pinning in a harness under test. The use of an LCD screen to display the status of a harness ensures faults are easily understood and displayed in the ECHTS, while providing a more comprehensive communication of detected faults compared to conventional testing and/or measurement systems. Compared to conventional systems, the ECHTS showed an improvement of testing times for a 1:1 and a one-to-multiple connector configuration, to 73% and a 15%, respectively, and a short operator's learning time.

Keywords

microelectronics system design; electronics system testing; cable harness; electronic circuit design

1 Introduction

Automation plays an increasingly important role in modern manufacturing industry as it offers a cost-effective way for a manufacturing enterprise (ME) to maintain market competitiveness in a highly globalized business environment. MEs depend heavily on automated processes aiming to deliver high quality products at high production rates, while keeping the production costs low[1, 2]. Several MEs, including those that manufacture electrical cable harness systems, still rely on a high input of manual work despite the advances in automation, largely due to the magnitude and complexity of processes involved in assembly of cable harnesses [3, 4].

Electrical harnesses (*aka.* wire harness, wiring harness, cable assembly, wiring assembly or wiring loom), an assembly of electrical cables/wires that transmit signals and/or electrical power, with the cables normally bound together by a durable isolating material and manufactured with a terminal, are used in many industries and applications (*e.g.,* aircraft or automotive electronic systems) to connect electronic components together [5]. In some applications, the pin configuration is not always 1:1, where the conductor at one end of the assembly connects to the same pin number on the other end, and some harnesses are terminated using different connector types at either end of the cable. Regulatory bodies and standards exist for cable and wire harness acceptability, such as the IPC/WHMA A-620 standard [6], which are used for quality assurance dependent upon the classification and area of use for the assembly. All harness assemblies must be tested prior to implementation to detect any defects. Owing to the predominantly manual fabrication process common manufacturing defects include an open- and short circuit and misconnection faults, all of which can, potentially, be screened and eliminated by using a test board apparatus to measure the harness' electrical capabilities and ensure its quality and functionality[7] as, for example, reported by Bi *et. al*[8, 9] for a limited number of conductors and implemented on the Allen Bradley programmable logical controller (PLC) board.

At present, only a few MEs have been able to embrace, with limited success, the automation of manufacturing, fabrication and testing of electrical harnesses. This is due to manual production providing a more cost-effective method for fabrication of these complex industrial products, especially for small batch sizes[1, 2, 8]. There are a variety of cable harness testing systems available on the market, including Cami Research's CableEye®, Cirrus Systems®, Molex®, SYNOR®, and others, which cater to a large number of configurations and have extensive testing methods. These systems tend to be designed to support known harness architectures and larger cable harness bundles. There is a demand for individual cable assemblies, cladding and wire terminations to integrate with the specific, custom-made electrical systems in the dynamically changing market - a demand that makes the testing of custom-manufactured harnesses using commercial solutions a challenging task for small and medium MEs, which often rely on mechanical test systems, each suited to a specific cable assembly termination. MEs often require an adaptable cable harness test system in order to reduce maintenance and testing times associated with manual and mechanical testing systems, a requirement that commercial harness testing manufacturers are often unable to address.

This paper presents the design, principles of operation and implementation of a low-cost automated electrical cable harness testing system (ECHTS), capable of testing cable harnesses to identify assemblies with open circuit, short

circuit and misconnection faults. Medium and small MEs often employ physical examinations of individual conductors in a cable harness system through the use of manually operated rotary switches and light emitting diodes (LEDs), which are an error-prone and time-consuming process. Through the use of a micro-controller, the ECHTS has been designed to efficiently test cable harnesses consisting of up to 32 conductors of any configuration and any termination type. Additionally, the system can be expanded to test up to 64 conductors and includes the ability to identify faults such as short circuit, open circuit, and mis-wired conditions in an electrical harness assembly.

2 Cable harness design and testing requirements

2.1 System protection requirements

One of the biggest threats to electronic systems is electrostatic discharge (ESD), a phenomenon in which a material becomes positively charged [10, 11], and which is known to cause, on average, 27% to 33% loss of products where integrated circuit (IC) components are present [12, 13]. The ESD effects on electronics occur due to direct discharge to an electronic component or equipment housing and indirect discharge on the equipment. ESD is generally classified using three main models, namely:

a) a human body model (HBM), which represents the human body discharging the current into a grounded IC,
b) a machine model, which represents a discharge from charged machines into a grounded IC, and
c) a charged device model, which represents discharge from self-charging ICs or devices during manufacture that come into contact with a grounded piece of equipment.

The most commonly used model for ESD is the HBM. An equivalent capacitance of 100 pF and an equivalent resistance of 1500 Ω is used to sufficiently represent the human body in the HBM model. A HBM ESD event has a typical rise time of between 6 and 9 ns, with a peak current pulse through a 500 Ω resistor of 463 mA for a pre-charged voltage of 1000 V. Depending on relative air humidity and clothing material, the charge which a human body can see typically ranges from 20 – 30 kV [14]. An electrical cable harness system design is therefore required to minimize the adverse HBM effects.

In microelectronics, active components of ICs are interconnected through layers of conductive thin-film metal, known as metallization, on the surface of the device [15, 16]. Metallization burnout occurs due to an injection of an ESD pulse, which can cause the metal to melt and subsequently cause open and short circuits on the device. Prior to metallization, several layers of silicon dioxide, SiO_2, are deposited on the device's surface. Failure due to ESD can occur through a disturbance to the breakdown voltage of SiO_2 isolation, known as oxide punch-through [17], which can cause shorting in the circuit. The susceptibility of the designed device is dependent on the thickness of the oxide layers, with failure most likely in thin layers of oxide [17]. Junction burnout occurs when an ESD transient has a magnitude high enough to initiate secondary breakdown, causing a high reverse leakage. A technique called "buffering" is often employed in testing systems as a method of ESD protection. This often involves adding resistance in series in a digital or analog circuit in order to provide a buffer for the current going to an alternative current loop established by an ESD protection device such as a semiconductor [18, 19]. ESD buffering elements serve the purpose of lowering current flow through the signal path, lowering voltage at the node through a resistor-divider network, and through the impedance matching of signal pins [19].

2.2 Requirements for electrical cable harness testing

An automated test equipment (ATE) is a system which, in general, tests some form of device or system in an automated manner. This can include the testing of ICs and circuit boards. Typically, the ATE system applies some form of stimuli such as an electrical signal to the device under test and verifies the operation of the system based off the response, such as the voltage or current seen. This test usually results in a "*pass*" if the device is working to the design specifications, or a "*fail*" if the expected response has not been received within some given tolerance [20, 21]. The ATE often involves a microcontroller to provide direction to the operation of the system. Process variables in the design of a cable harness include the terminal and connector type, and wire length, gauge, colour and marking [3, 5].

A connection test prior to application can eliminate failure of equipment due to short or open circuits and improper connections [22, 23]. There are numerous causes for defects in a cable harness assembly. The quality of a solder joint which connects the pins to connectors is dependent upon factors such as the correct type and amount of flux,

suitable heat and time, and correct solder amount. If heat is too high or prolonged, the solder can penetrate the wire and underneath the insulation which weakens and reduces the amount of solder on the joint. If this joint detaches, an open circuit will be present in the conductor. Alternatively, insufficient heat will cause cold solder joints in which the conductor and solder do not form together properly, which can leave the joint susceptible to defects such as cracking [22, 23]. The compromise of insulation on individual wires can lead to defects in a harness assembly. As a force is applied to the wires, such as bending, flexing, or vibration, the conductors can become isolated by an airgap, effectively resulting in physical contact with each other. This leads to a short-circuit in the assembly, which may also result from age where insulation is compromised or degraded. Open circuits can be caused by a variety of sources, such as improper mating forces, poor crimping in the assembly, contaminated contacts or improperly seated pins [22, 23]. Human error is another source of defect, which can lead to the incorrect pinning of conductors in the connector.

The IPC/WHMA A-620 standard [6] for requirements and acceptance for cable and wire harness assemblies details the necessary tests in which to measure quality. Two essential tests for Class 3 assemblies, which includes harnesses for use in high performance electronic products, are the continuity and shorts tests. The standard requires the continuity to be whichever is greater of 2 Ω, or 1 Ω plus the maximum resistance which is specified of the wire [6].

3 Implementation of the proposed testing system

3.1 ECHTS structure

Methods to reduce the risk of human error in the testing process were investigated empirically. The technical team at the company were consulted and it was determined that the use of LEDs became confusing in fault conditions. To minimise confusion, a liquid crystal display (LCD) display was chosen to provide a detailed description of any faults detected in the harness-under-test. Additionally, LEDs were chosen as a second-line-of-defence to provide a "*pass*" or "*fail*" indication.

Continuity testing includes the determination of short-, open- and mis-wire faults in the harness under test. The proposed ATE tester for ECHTS has been envisaged to be capable of initially testing up to 32 points, with the ability to be expanded up to a 64-conductor harness. Table 1. shows the developed initial test specifications prior to the design stage, including perceived 'ideal' testing time of 10 s or less for improved user satisfaction. It was determined that the proposed ECHTS would compare harnesses for testing to a known good cable harness. The use of pushbuttons was decided to enable user control of both the learning of the known good cable harness and subsequent readings of harnesses-under-test.

The circuit required multiple input/output (I/O) pins for the function of various sub-circuits. Consequently, the control system was implemented using an Arduino Mega 2560 R3 microcontroller board. The Mega is based on the ATmega2560, a high performance and low power 8-bit Atmel microcontroller. The Arduino Mega provides 53 digital I/O pins and 15 analog inputs, with a recommended DC current of 20 mA per pin. Additionally, the microcontroller contains inter-integrated circuit (I2C) protocol and serial peripheral interface (SPI) communication. Arduino microcontrollers accept various sources of power including via USB and power jack, with a maximum input voltage of 7 - 12 V DC. A common 9 V AC-DC power supply was selected for the input power to the system due to their prevalence and low cost. Battery operation was considered unnecessary in the company, since the majority of testing took place on a specific test bench.

The design ATE required each conductor in a harness assembly test to use a digital pin per output to its individual circuit line and an analog input to the microcontroller. To enable the initial 32-way harness specified, a total of 64 pins would be required using standard general-purpose input/output (GPIO) pins. For the specified expansion ability, 128 GPIO pins would be required. To resolve this issue, two options were considered: an expansion shield, and a daisy-chain of shift registers to act as a bank of outputs using the SPI bus. The daisy-chain shift register method, shown in Figure 1, was chosen for the design simplicity, ease of integration and cost considerations. This method reduced the required I/O GPIO pins on the ATE microcontroller by providing output to 64 lines using four outputs.

Table 1 ECHTS initial design specifications

Test Specifications	
Test Voltage	5 V
Test Current (max)	10 mA
Test Time	< 10 s (total)
Test Points	32 points; expandable
Short Circuit Test	Yes
Open Circuit Test	Yes
Mis-wired Test	Yes
Resistance Test	No
Physical Characteristics	
Weight	< 4 kg
Size (max)	30 x 15 x 15 cm
Power Supply	
Input Voltage	90 – 264 V AC
Output Voltage	9 V DC
Output Current	1 A
Output Power (max)	9 W
Over-Voltage Protection	Yes
Over-Current Protection	Yes
Short-Circuit Protection	Yes
User Interface	
Display	16 x 2 LCD
Status Indicators	RGB LEDs
Switches	Learn button, read button
General	
Calibration	Not Required
Computer Requirements	Required for modification only
Battery Operation	No
Environmental	
Operating Temperature	Ambient
ESD and Transient Protection	Yes
External Components	
Connection Method	Connector Board
Expansion Module	Yes

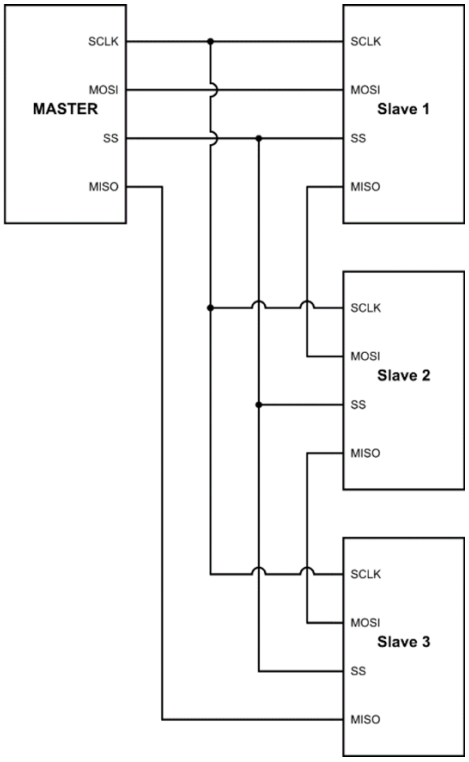

Fig. 1 Master-Slave SPI in daisy-chain configuration; the logic signals of the SPI bus include Master In Slave Out (MISO), Master Out Slave In (MOSI), Slave Select (SS), and Serial Clock (SCLK).

I2C is a is multi-master protocol which operates via two signal lines. The benefit to using I2C in this ATE design was a reduced requirement for microcontroller pins, reduced logic and the simplification of the overall PCB design. The two signal lines of I2C, serial data (SDA) and serial clock (SCL), can connect multiple slaves and masters, shown in Figure 2.

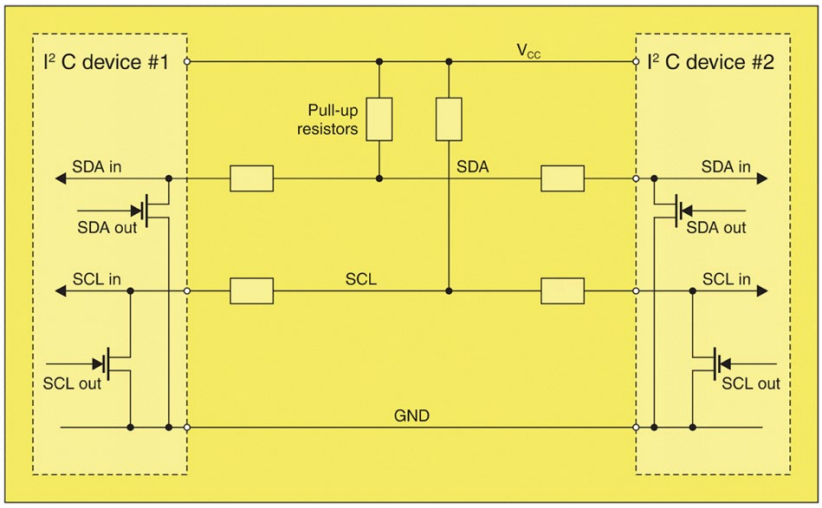

Fig. 2 I2C device connection; image adapted from [24]

The Adafruit RGB 16 x 2 character LCD shield was chosen for the user interface's display due to its ability to operate via I2C. This was achieved through the use of an MCP23017 port expander on-board the shield, which also allows the LCD shield to incorporate four directional pushbuttons and a select pushbutton. A 16 x 2 display was ideal for the small dimensions required. However, this compromised the ability to display multiple faults, if

present, to the user. The Adafruit LCD shield's directional pushbuttons enable scrolling through multiple lines of faults when required. Additionally, the select pushbutton allows the user to begin "*learning*" a new "*golden*" harness, as well as functioning as a "*read*" button to begin subsequent tests.

Figure 3. shows the conceptual ATE design of the user interface and driver circuits. A serial-to-parallel shift registers feed the test circuit the sequential voltage through the use of the SPI protocol. The output of the test circuit is fed into the switching circuit consisting of cascaded parallel-in-serial-out multiplexers. Three select lines are used for the control of the first line of multiplexers, which are sent to the ADC for reading and comparison.

Methods of ESD protection were investigated to identify the most robust and practical solution for the circuit. In the selection of protective solutions, consideration was given to the number of protection circuits required. The test circuit consists of 32 repeated lines, one for each conductor of the harness-under-test. Additionally, the final printed circuit board (PCB) could not exceed the mechanical constraints of the enclosure. Consequently, the circuit was designed with consideration given to the minimization of components.

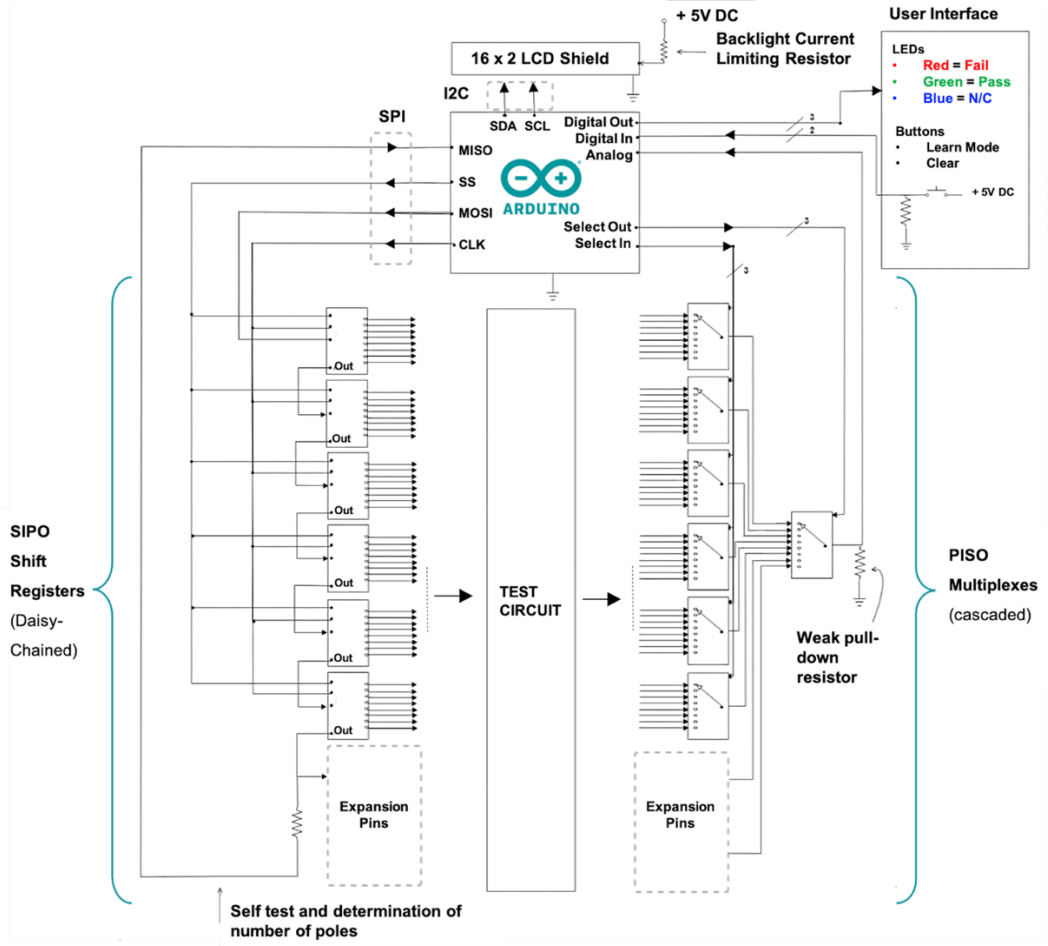

Fig. 3 ECHTS conceptual design of the user interface and driver circuits; shift registers include Serial-in, Parallel-out (SIPO) and, multiplexers include Parallel-in, Serial-out (PISO).

The mechanical constraints of the system's enclosure dictated the protection method which was chosen. Robust clamping circuits offer high protection. However, these methods were considered too costly to implement into 32 lines of the circuit. These methods would have also occupied valuable space on the final PCB design.

For ESD protection, a Zener diode [25, 26] was chosen at both inputs and outputs of each circuit to protect against ESD discharge caused by the contact occurrence when plugging in a harness for testing. If an ESD strike occurs without ESD protection, all current from the strike is allowed to flow directly into the sensitive components of the

circuit. When a strike occurs and there is a protection diode present, the high-voltage occurrence will cause the diode to breakdown, providing a low-impedance path for the current to ground. This facilitates the protection of the circuitry downstream of the diode [26].

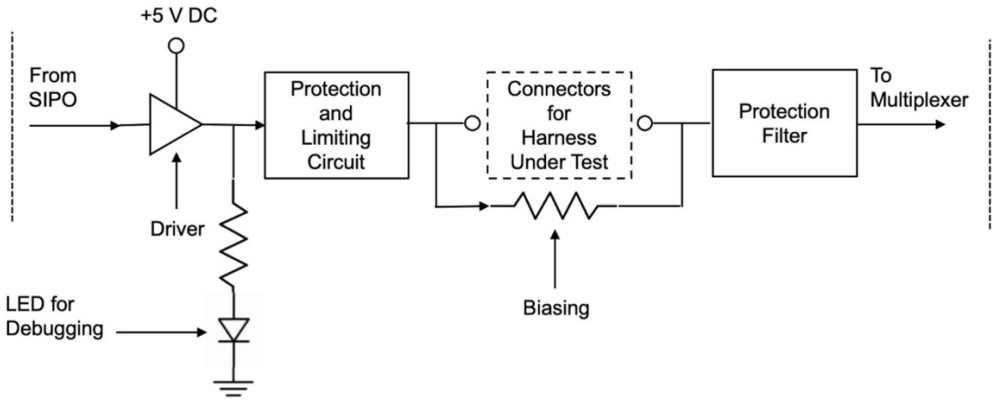

Fig. 4 ECHTS driver and test line circuit

A test current of 10 mA was considered sufficient due to the short length and small resistance of the conductors under tests. A 74HC595 shift register is limited to a 6 mA per output pin at 5 V DC. To achieve the desired 10 mA test current for the system, the use of a P-channel metal-oxide semiconductor field-effect transistor (MOSFET) was chosen for switching control of the circuit. MOSFETs were chosen in favour to bi-polar transistors due to their lower voltage drop, ability to handle larger currents in general, and their low draw of gate current from the microcontroller pins [27, 28]. The shift register outputs supply the gate of a P-channel MOSFET and when a logic "*0*" is present at the gate of a P-channel MOSFET, the MOSFET enters the saturation region and is switched to its "*on*" state. At the input side of the circuit, the voltage through the selected P-channel MOSFET provides 5 V DC. The protection diode selected for the input side of the circuit was subsequently selected to clamp at slightly above 5 V. This led to the selection of a 5.1 V Zener diode. The value of the buffering resistor was chosen to ensure that the voltage-to-current relationship was satisfied and ensured the maximum current rating of the Zener diode was not exceeded. A 150 Ω surface mount device (SMD) resistor was chosen with a power rating of 500 mW. A gate current limiting resistor was implemented into the circuit prior to the input of the MOSFET gate. To determine the drive current required from the shift register output into the gate, the Eq. 1

$$I_{gate} = C\frac{\delta V}{\delta t} \tag{1}$$

was used, which related the desired current, I_{gate}, to the output capacitance, C, on the shift register pin to voltage level, δV, change from logic 1 to logic 0 in the time domain, δt, of the rise time of shift register. It was determined that the drive current required was approximately 5 mA.

A pull-up resistor was placed between the positive-channel metal oxide semiconductor (PMOS) gate, shift register output and supply voltage to ensure floating pins were not present. The resistor prior to the Zener diode was calculated to ensure the dissipated power of MCU0805 thin-file resistors did not exceed the required maximum power dissipation of 0.2 W. The value closest in standard values was determined to 150 Ω. The LED indicator for each line was chosen to be driven by a 2 mA current. This value was determined to be high enough to provide an acceptable brightness from each LED for the user. The forward voltage of the chosen LED was 2.4 V and the resistor was subsequently calculated to be approximately 1.3 kΩ. This value was changed to 1 kΩ to reduce the number of variations in the circuit and reduce materials cost. The resulting LED current was slightly higher at 2.6 mA and provided acceptable light emission for a user and debugging purposes.

To determine the step size of the 10-bit analog-to-digital (ADC), the number of levels of the ADC were calculated using Eq. 2

$$\Delta = \frac{R}{2^b} \tag{2}$$

which related the step size of ADC, Δ, to the sample voltage range, R, change relative to the number of bits, b, and

was determined to be 4.9 mV. Each conductor of a harness assembly was assumed to have a resistance of 2 Ω or less. By placing a biasing resistor in parallel to the connection points of the harness under test, a known value at the ADC for the open circuit condition can be detected in the absence of a conductor's connection. The value of 10 kΩ was chosen as this biasing resistor in order to fall within the resolution of the ADC and provide an acceptable result. To ensure the series resistance of the circuit was maintained at approximately 500 Ω in order to satisfy the specified 10 mA test current, a 330 Ω resistor was chosen as the shunt resistor in the attenuation circuit prior to the protection capacitor. The remaining resistance of 150 Ω was placed in series to form an attenuator circuit. The circuit calculations for components were considered in the time domain. A first order low-pass filter was placed prior to the input pin on the microcontroller. A capacitor value of 160 nF was calculated using Eq. 3

$$C1 = \frac{C_{ESD} \times V_{ESD}}{V_{Final}} - C_{ESD} \tag{5}$$

which related the capacitance of an ESD event, C_{ESD}, voltage of an ESD event, V_{ESD}, to the desired final voltage, V_{Final}, to form the RC filter. A common capacitor value of 100 nF was chosen to maintain a similar result to the calculated value while ensuring the chosen values aligned with company standards and maintained cost efficiency. This value was verified through simulation. The RC component was placed prior to a clamping diode to further attenuate an ESD event, which was selected to be a 4.7 V, 500 mW Zener diode. This value ensured clamping occurred higher than the test voltage under normal operating conditions. The circuit was simulated using LTSpice [29]. These values were seen to satisfy the circuit requirements with a test current of 10.6 mA and a voltage level of 2.74 V seen at the input to the ADC. It was determined that the circuit values were acceptable and provided test values within the range of the ADC resolution.

Figure 5. shows an ESD event simulation model using LTSpice [29]. The ESD event was modelled using the HBM which consisted of a 100 pF capacitor and a 1500 Ω resistor. A voltage source of 8 kV was set to charge the capacitor by modelling the event using a rise of 0.6 ns in accordance with HBM parameters.

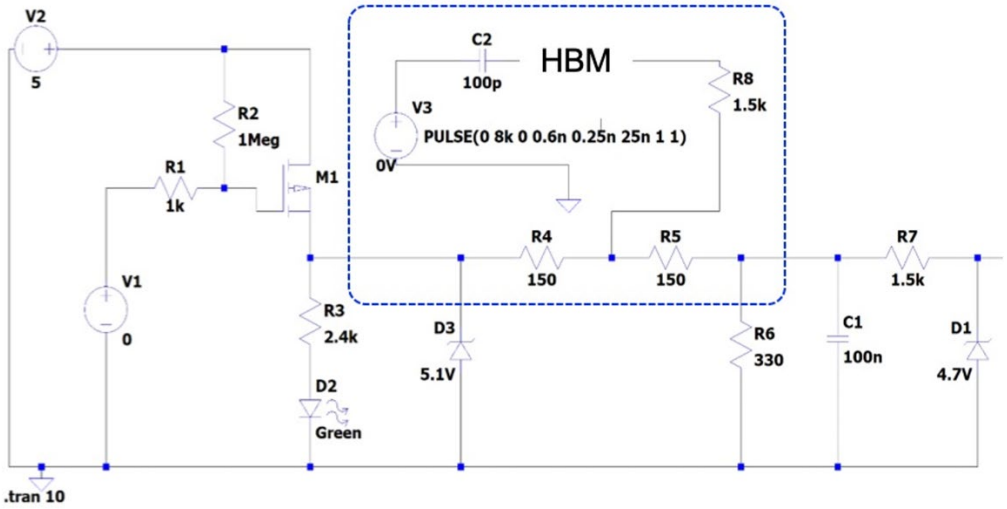

Fig. 5 HBM ESD event simulation circuit

A peak current of 3.6 A was seen across the capacitor C2. This value attenuated to approximately 1.7 A at the point of injection across resistor R5. The low pass filter and Zener diode performed to an acceptable level where the current prior to entering the ADC was seen to be approximately 8 μA due to the RC filter providing a low impedance to ground. The voltage injected into the circuit through simulation was approximately 155 V, with an attenuation circuit and clamping diode preventing voltages over 4.7 V from entering the analog input pin of the microcontroller. The voltage seen at the input side of the circuit was seen to be approximately 5 V. It was concluded that the selected values for the circuit were sufficient in providing protection against an ESD event within the HBM guidelines.

3.2 Power supply circuit design

The ATE microcontroller requires a 9 – 12 V DC supply, for which a 9 V AC/DC power pack was chosen. The design of a power supply circuit must consider protective mechanisms and prevention strategies to protect the system from faults. To prevent reverse polarity, a diode was used to isolate the circuit from the supply. The diode functions as though it were an open circuit when in a reverse polarity situation and prevents current from conducting when the cathode voltage of the diode is higher than the anode voltage [30, 31]. The voltage provided from the AC/DC adapter was required to be stepped down to a 5 V DC voltage for the MOSFETs and user interface components. To regulate the power supply, an LM805 linear regulator was incorporated to the design. The linear regulator provided a step-down voltage of 5 V DC, while also serving to reduce any ripple on the power supply with its ripple-rejection capabilities. Decoupling capacitors were added to the regulator to reduce any remaining ripple on the line and improve transient response. A value of 0.1 μF was chosen with consideration given toward the datasheet recommendations and company standards. The regulated 5 V DC supplies the main circuit and the user interface. Capacitors were placed on each power rail for smoothing and reduction of ripple. This value was chosen as 100 nF to align with company standards.

To determine the heat dissipation of the linear regulator and verify whether a heat sink was necessary in the system, the total load current of the system was approximated. The power dissipation of the LM805 was used to determine whether the system would need a heat sink to prevent overheating. The LM805 datasheet specifies a junction to ambient thermal resistance, $R_{\theta JA}$, as 23.9 °C/W and a maximum junction temperature of 150 °C. It was determined that the calculated values were within the limits of the datasheet recommended values and a heat sink was not necessarily due to the tester being used briefly at any given time of operation and would require considerably less current than the maximum output current of the voltage regulator. Figure 6. shows the block diagram of the power ECHTS supply circuit components.

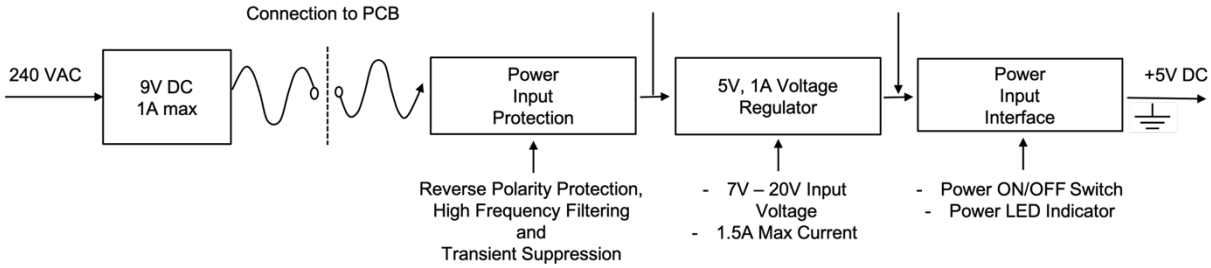

Fig. 6 ECHTS power supply circuit components

3.3 Control program for testing

The software was developed during the manufacture of the PCB using the Arduino integrated development environment (IDE) [32]. The Arduino IDE is an open-source software for Arduino compatible development boards. Arduino was selected as the microcontroller development board for this design due to its low cost, prevalence, and free software which removed the need for additional software to be purchased for the implementation of the design.
Figure 7. shows the flowchart of the software implemented for the system. The three design specifications which testing must identify are the short circuit, open circuit and mis-wired conditions. Initially, the system does a "*self-test*" by presenting all circuit lines with a voltage. This turns all LEDs on in the circuit and verifies the correct functioning of the shift registers.

At the beginning of the test procedure, the program waits for the closure of the "*SELECT*" button on the LCD shield to commence the learning function. To "*learn*" a known good harness, a test sequence is sent through the shift registers using a "*walking ones*" pattern, while the voltage is received on "*End B*." The multiplexer selects lines S0, S1, and S2 loop through lines 1 through 8 for each test pattern applied to the shift registers. The select lines S3, S4 and S5 select multiplexers 1 to 4 at every 8th iteration and reads this information in a 32 x 32 2D array through an analog GPIO pin. The process is repeated for subsequent harnesses inserted for testing, with the test array values being compared to the known good harness values. The system displays a brief description of the harness it has learned through indicating the number of conductors detected, and whether the harness is a 1:1 configuration or a one-to-multiple configuration.

The first test determines if a voltage is detected at the incorrect End B pin. If this condition is detected, the system

stores the test line as a mis-wired fault line. If there is no voltage received on the intended End B pin, and no voltage is received on any other pin, the line is recorded as an open circuit. The End B pins are then read to determine whether multiple pins present a "*pass*" voltage. If there is only one pin intended to receive the voltage and multiple pins are detected as receiving the voltage, the system records a short circuit fault on the multiple lines.

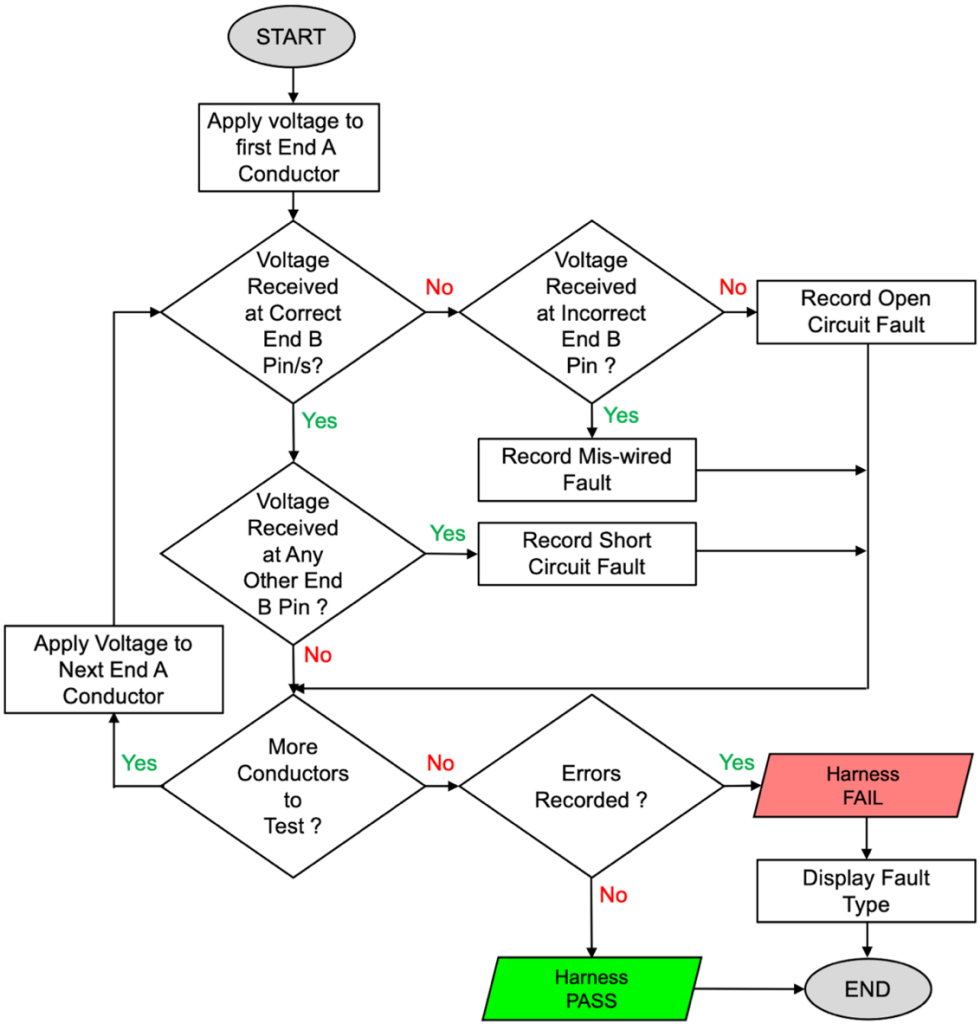

Fig. 7 Flowchart of ECHTS software logic

The final schematic design of the ECHTS is shown in Figures S1 – S3 (Supplemental data), including the schematics of the ECHTS final main system (Figure S1), the individual conductor test circuit (Figure S2) and the connector board schematics (Figure S3). A multi-sheet design was chosen in order to simplify the schematic design process.

4 Software simulation and ECHTS prototype testing

During the manufacture of the ATE PCB board, the simplified version of the final design was implemented on a breadboard and tested in order to classify all cases of fault conditions in ECHTS appropriately. The results of the software displayed a test program which could identify multiple faults within the harness under test with accuracy. Multiple faults were presented to the ECHTS prototype, including an open circuit, mis-wiring, two-wire short circuit and a three-wire short circuit. All conditions were successfully detected by the software. The system was compared with the Molex® Harness Tester, which is the most commonly used tester at the company. The program was efficient, with test times falling under 2 seconds for a 16 GPIO conductor test, excluding set-up time. The design of the final PCB board incorporated multiple test points to facilitate ease of testing. Test points can be seen

on Figure 1(S) and 2(S), which show the schematic for all main board circuits. The test points are denoted by the designator "TP." It was expected that the input voltage being provided to the individual points of the test circuit after the driver circuit would be approximately 5 V DC. Additional test points were placed on SS, SCK, MOSI, MISO, SDA and SCL communication lines for debugging purposes.

The final ECHTS design was tested and its performance was compared to the Molex® Harness Tester, a system that is most commonly used by small and medium MEs, with the first test conducted using 10-way Molex® harness assemblies, which were not in a 1:1 configuration. To evaluate the ECHTS performance, untrained ME operators were selected and requested to perform 5 individual tests using each system, the Molex® and ECHTS. The systems were then compared when testing a 10-way harness with a 1:1 configuration. Additionally, ME operators were screened when conducting another 5 tests on each system using the 1:1 configured Molex® harness. Each system test was timed during the testing, and testing times are collated in Table 2.

Table 2. Testing time (in seconds) for Molex® Harness Tester compared to the designed ECHTS

Test Number	Molex® Harness Tester (Any)	ECHTS (Not 1:1)	ECHTS (1:1)
1	23	25	8
2	25	22	9
3	24	19	8
4	25	23	7
5	27	16	9
Average	*25.25*	*20*	*8.25*

The average test time for a single test was determined from the data and it showed that the ECHTS improved testing times by approximately 15% when compared with the Molex® Tester system in the case of testing harnesses which are not 1:1 configured. The 1:1 configuration testing times were significantly lower compared to the Molex® Tester, with a 73% reduction of test time. Each system was then timed for testing five tests total. It was determined that the average time for testing 5 cable harness assemblies on the new system was 53 s, while the Molex® Tester took 101 s for the same test. This equates to a 47% improvement in test times when using the designed ECHTS for 1:1 configuration tests. The average test times for each system can be seen in Figure 8.

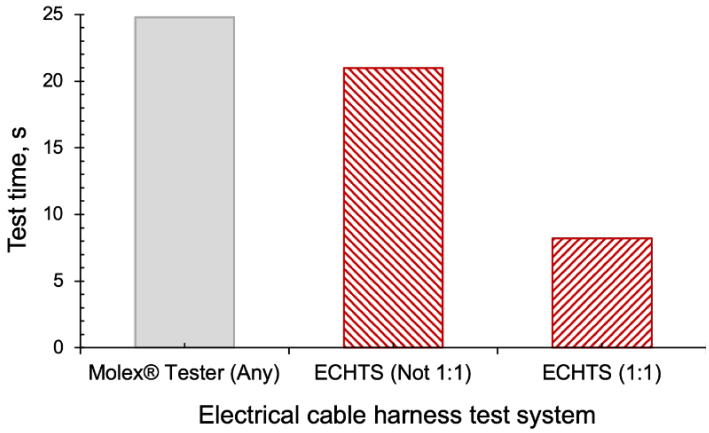

Fig. 8 Testing times of the ECHTS compared to Molex® electrical cable harness test system

The ECHST displayed faster performance compared to the Molex® Tester in testing a harnesses which were not a 1:1 configuration. Additionally, the testing times of 1:1 harnesses were significantly reduced using the ECHTS with times per-test of approximately 8 s compared with the Molex® tester which averaged at approximately 24 s. To determine the perceived usability of the ECHTS, trained operators skilled in electrical harness assembly, handling and testing were selected to test a random electrical harness and rate the ECHTS on a scale of 1 to 10 for its ease of use, with 1 being the lowest and 10 being the highest rating. It was determined that the ECHTS had a usability rating of 8.7/10. Additional screening was conducted to determine the learning time required to operate

the ECHTS, by ME operators, which were not experienced in operating ECHTS. The screening results showed that it took under 60 s for each untrained ME operator to learn the ECHTS prior to conducting tests, which signifies its user-friendly design and simplicity of operation.

5 Summary and conclusions

A functional and efficient automated electrical cable harness testing system, ECHTS, as detailed in this paper, with the capability of testing numerous cable harness configurations was designed and successfully implemented. The ECHTS displayed significantly reduced testing times and improved cable harness testing accuracy compared to a common Molex® Tester commercial cable harness testing system and packaged in a more user-friendly design. The ECHTS is capable of testing up to 32 GPIO conductors in a cable harness and allows an additional 32 GPIO conductors to be tested through the use of an expansion board. The ATE user interface was found to be intuitive and negates a lengthy learning curve for operation by the user. User satisfaction for ECHTS was determined to be 8.7 on a 10-point satisfaction scale with user learning times under 60 s.

An interchangeable GPIO connector for the harness adapters allows the ECHTS to test any cable harness required, provided the connector types can be mounted and the harness size and specification is within the limits of operation. Three lines of defence were employed for fault detection including LEDs per conductor line, a status LED with a pass/fail indication, and an LCD display with a description of any faults detected. The ECHTS is capable of detecting open circuit, short circuit and incorrect pinning in a harness under test. The use of an LCD screen to display the status of a harness ensures faults are easily understood and displayed, while providing a more comprehensive communication of detected faults compared to common commercial ATE for electrical harness systems. This is an improvement over previous testing systems/methods used at the company, which were ambiguous in displaying faults through the use of LEDs.

The ECHTS was found to improve testing times significantly. Namely, the testing of harnesses in a 1:1 configuration achieved a 73% reduction in test times. In the one-to-multiple configuration, an improvement of approximately 15% in test times was achieved for the ECHTS. Additionally, the designed ECHTS was found to reduce testing times when multiple cables are to be tested by approximately 50%.

Cable harnesses are used extensively within the global market, with applications in industries such as automotive, aerospace, aviation, military, medical, telecommunications and audio. The ECHTS detailed in this study provides a solution for effectively testing harnesses used in various industries with the system’s ability for universal configuration. Additionally, the system has the capacity to be used as a tester for various components such as diodes, motors, loudspeakers and inductors.

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Conflict of interest

The authors confirm that there are no known conflicts of interest associated with this publication and there has been no significant financial support of this work that could have influenced its outcome.

Ethics

The authors confirm that material presented in this publication is exempt from formal institutional review and/or national ethical committee approval.

Author contributions

PMPK and MJW designed and conceptualised the study. PMPK developed research methodology, carried out the experiments, data collection, developed the theoretical formalism, analysed the data and drafted the manuscript. MJW and MR coordinated and supervised the study. CB managed the project and provided funding and resources for the study. MR drafted and critically revised the manuscript. All authors read, commented on previous versions of the manuscript, gave final approval for publication and agree to be held accountable for the work performed therein.

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