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Low power ROM Employing Dynamic Threshold-Voltage MOSFET (DTMOS) Technique

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Abstract-This paper examines the performance of two 128-bit ROM circuits, implemented on Silterra 0.18 μ m CMOS process. The first circuit is built using standard NMOS transistors, runs on 0.9V supply voltage, has gate voltage of 0.45V and consumes 102.07 μ W power. The second circuit is designed partly using Dynamic Threshold-Voltage MOSFET (DTMOS) transistors with the aim to minimize power consumption. It runs on 0.7V supply and has gate voltage of 0.35V. The DTMOS approach is implemented on the 128-bit ROM core and in the pull up circuit of the column decoder. The latter ROM circuit's power consumption is 38.93 μ W, 61.86% less than the former, at the expenses of larger die area due to the usage of deep n-well process. The standard and DTMOS circuits have the die areas of 0.139 μ m² and 0.235 μ m², respectively.

I. INTRODUCTION

Digital mobile devices are becoming more commonplace than ever, with users demanding more performance such as longer battery life, bigger storage capacity and bright and colorful display. Submicron technologies allow ICs to have smaller footprints, making mobile devices more compact and have smaller form factors. Designers have tackled the form factor issue, but they now have to contend with power consumption. Lower power consumption means minimized power dissipation, and to achieve this, ICs need to be supplied with lower voltage. Besides, lower voltage requirements allow devices to be powered with smaller and lighter batteries.

There are many researches that focus on achieving lower power consumption for various

analog devices, but not as much work is done on digital devices. Focus should be given on digital devices too, as they are a main contributor to the growth and development of the modern world technologies. Many digital devices have ROM (Read Only Memory) blocks as part of their circuits. ROM blocks consume lots of power because they have highly capacitive lines and are frequently accessed. Reducing power consumption in these lines has been the main objective of several research groups and they have proposed some techniques. Mooney et al propose lowering the number of transistors in the ROM core [1], while others propose lowering the swing voltage of the bit lines [2]-[7]. So far, there is no proposal to employ DTMOS technique for low voltage usage in a ROM.

Dynamic Threshold-Voltage (DTMOS) technology has become more popular among circuit designer in recent years. This paper examines DTMOS' features that do not involve complex circuits or changing the basic process. DTMOS has low leakage current when reverse biased, and higher current drive (lower threshold voltage due to forward bias body effect) when switched on. Its implementation effects the transistor bulk connection that tied with its own gate.

In the second part of this paper, both standard NMOS and DTMOS-based NMOS are presented and their circuit characteristics are analyzed. The third section of this paper compares and contrasts all the components of the power consumption of standard 128-bit ROM (128SR) and DTMOS-based 128-bit ROM (128DR). Finally, the last section contains further discussion and conclusion.

II. DTMOS AND CONVENTIONAL NMOS COMPARISON

Most of the early works on DTMOS focused on digital circuitry, with the potential to achieve lower power consumption through this technology. This has been demonstrated by two research groups, where one group designed a low-voltage (1-V) operational amplifier (Op-Amp) with 35.7 MHz unity-gain frequency and 64 degree phase margin under load conditions of 5pF and 10kΩ [8]. The other group fabricated a stable bandgap reference circuit using DTMOS transistors [9]. Suitable for low-voltage, low-power ICs which can tolerate moderate accuracy, the bandgap-reference circuit runs on supply voltages as low as 0.85 V and generates reference voltage of 0.65 V while consuming only 1 μW power. The die occupies an area of 0.063 mm² using standard 0.35-μm CMOS process.

DTMOS transistors operate in low power at very low voltage. The threshold voltage of the device is a function of its gate voltage. Whenever the gate voltage increases, the threshold voltage, V_t drops, resulting in a higher current drive, I_d compared to the standard MOSFET for low supply voltage [10]. DTMOS can achieve low leakage when it achieved Highest V_t at $V_{gs}=0$ and can achieve high speed when it achieved Lowest V_t at $V_{gs} = V_{dd}$ [11].

In a DTMOS circuit, the bulk is tied to its own gate as shown in Figure 1. This circuit can be observed from two angles [9]. First, the device can be viewed as a lateral bipolar PNP with an extra gate over the base. Second, the device can be seen as a PMOST with a dynamically regulated threshold – every change in V_{gs} causes a change in the threshold voltage. The device's name originates from this second view. The voltage drop in the silicon due to Φ_{Gw} as the barrier lowering voltage is denoted as Φ_{b1} . It can be stated that the drain current of a DTMOS is

$$I_D = I_0 \cdot T^\eta \exp \frac{q(V_{GS} + \phi_{b1} \pm V_{GAP,0})}{kT} \quad (1)$$

The barrier lowering voltage Φ_{b1} is given by:

$$\phi_{b1} = \frac{\phi_{GW} \cdot C_{OX}}{C_{OX} + C_{depletion}(\phi_{b1})} \quad (2)$$

The apparent material bandgap in the DTMOS is given by:

$$V_{GAP,apparent} = V_{GAP,0} \pm \phi_{b1} \quad (3)$$

A. Circuit Design

Conventional and DTMOS-based NMOS transistor basic circuits are designed using Mentor Graphics Design Architect and simulated on ELDO. Both designs use SILTERRA 0.18μ technology with the NMOS transistor width-length ratio of 5μm-0.5μm.

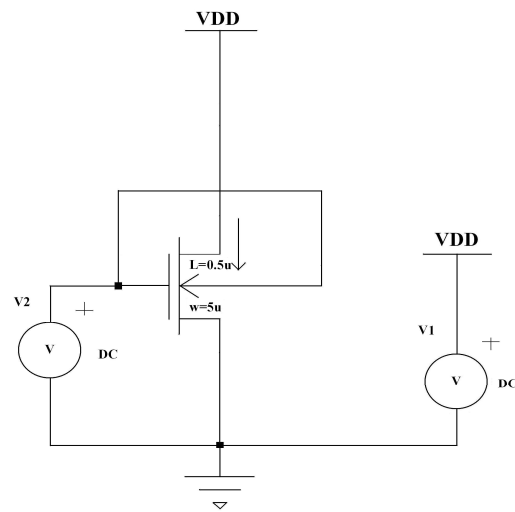


Figure 1: DTMOST-based NMOS basic connection

B. Result

Table 1 shows the simulation results for both conventional and DTMOS-based NMOS analysis. It shows that when V_g increased, I_d will also be increased. Meanwhile the threshold voltage, V_t is decreasing for both circuits. It is clear from the table that DTMOS-based NMOS possesses superior I_d at lower V_t .

Table 1 – Comparison

| Input and Supply voltage | | Nmos | DTMOS |
|--------------------------|----|-----------|-----------|
| Vg=0.5V, Vdd=1.8V | Vt | 0.16977V | 0.19459V |
| | Id | 8.0783uA | 39.0925uA |
| Vg=0.6V, Vdd=1.8V | Vt | 0.16829V | 0.19437V |
| | Id | 31.6822uA | 95.2259uA |

III. ROM EXPERIMENTAL AND SIMULATION PROCESS

Studies show that ROM cores dissipate most of the power because word lines and bit lines have a large number of cell transistors and bit lines that are selected for each access [12]. Furthermore, most of the power is dissipated due to switching of the bit lines [13]. DTMOS-based NMOS transistors have been implemented on 128-bit DTMOS ROM (called 128DR in this paper) core and in the pull up circuit of the column decoder. For comparison purposes, a 128-bit standard ROM (called 128SR in this paper) is constructed by using a conventional NMOS transistor.

A. 128-bit ROM Circuit Design

128DR and 128SR are designed using Mentor Graphics Design Architect, employing SILTERRA 0.18 μ technology (php, L=0.5 μ W=10 μ for PMOS. nhp, L=0.5 μ W=5 μ for NMOS) and simulated using ELDO. The different is at an NMOS transistor inside the pull up circuit connection of column decoder and inside the 128DR ROM core as shown in Figure 2 and Figure 3, respectively. Both have their NMOS bulk connected to their own gates.

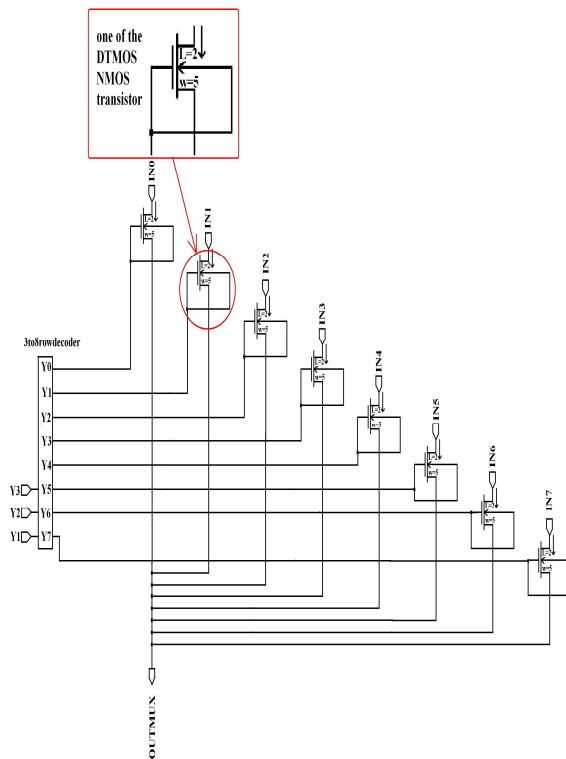


Figure 2: Inside pull up circuit of column decoder with the entire transistor use DTMOST-based NMOS

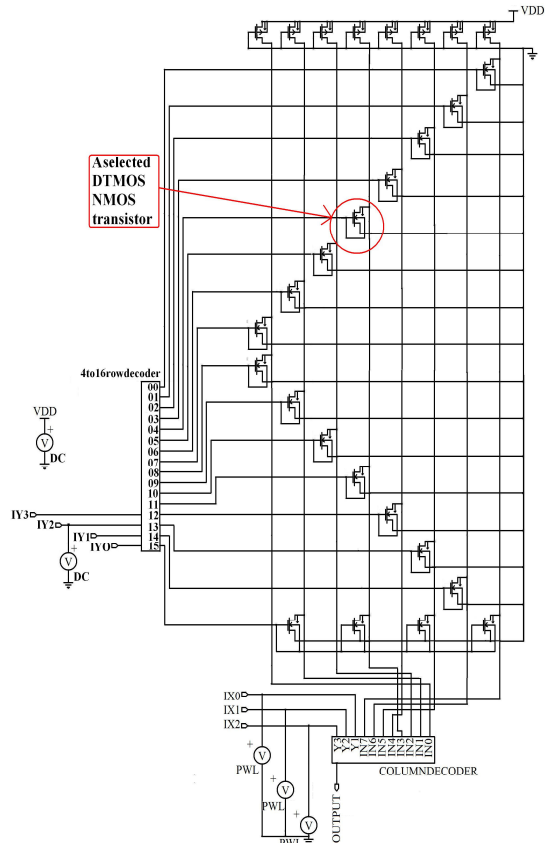


Figure 3: ROM core of 128-bit DTMOS ROM (128DR) which has DTMOST-based NMOS.

B. Result

In each simulation, the drain current at transistor of column 4 and row 5 are taken for comparison. A 0100 input is inserted at a row decoder. These inputs are referred to as gate voltage, V_g of the transistor. For the column decoders, a Piecewise Linear (PWL) analysis is injected so that the output voltage at the row 5 will swing from first column to the last column. An average drain current, I_d from both 128SR and 128DR circuits at the switched on transistors are taken to analyze their performance.

From the simulation results, only the minimum values of V_{dd} and V_g are picked for both circuits. These are the minimum conditions for the circuits to perform their operation correctly. The values are 0.9V and 0.45V for 128SR, and 0.7V and 0.35V for 128DR, respectively.

The top graph of Figure 4 shows the output voltage graph for 128SR, for the 0100 input at the row decoder. We can see the voltage drop at the row decoder.

during the PWL input at 61nS. The high input the top show the average drain current picked from column 4 and 5. The last 3 graphs is for the PWL input DC at IX0, IX1 and IX2. They show the output voltage waveforms from 0nS until 160nS for 000 to 111 inputs, respectively.

The top graph of Figure 5 shows the voltage output for 128DR at the 0100 DC input from row decoder. The last 3 graphs is for the PWL input DC at IX0, IX1 and IX2. The results are quite similar to the 128SR output graph. The second graph show the average drain current picked from column 4 and 5. The average drain current of both 128SR (Figure 4) and 128DR (Figure 5) circuits are 55.62µA and 113.41µA, respectively.

A unified active power consumption for ROM of M columns and N rows is approximately given by:

$$P = V_{dd} \times (I_{array} + I_{decoder} + I_{peripheral}) \quad (4)$$

In general, the power dissipation is dominated by the array [14], so the decoder current and the active power dissipation of peripheral can be negligible. From the equation given, the power consumption for 128DR circuit is 38.93µW and 128SR is 102.07µW.

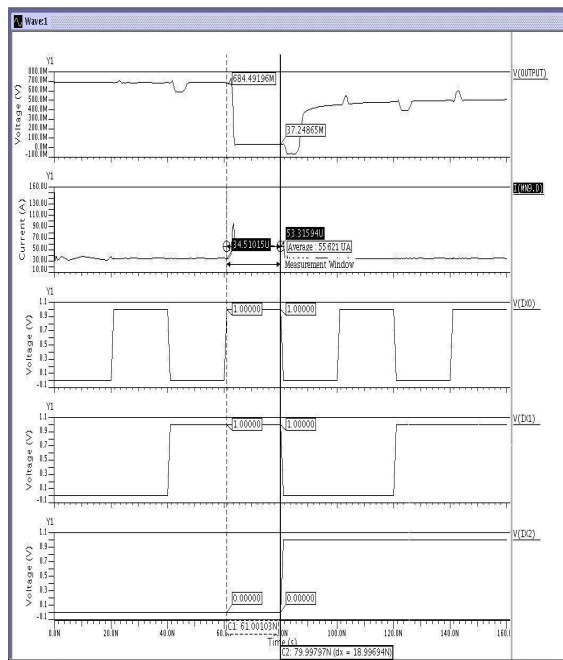


Figure 4: Overall graph that have ROM output, drain current, Id and input(IX0, IX1, and IX2) for 128-bit standard ROM at transistor column 4 row 5

represents a 0.45V value. The second graph from

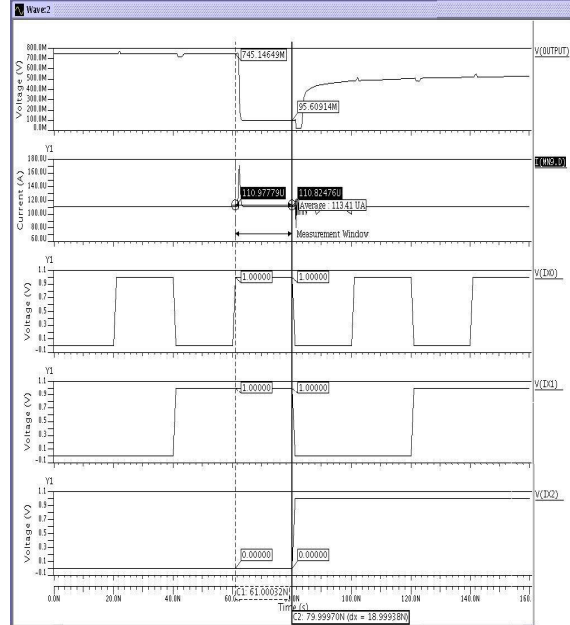


Figure 5: Overall graph that have output, drain current, Id and input(IX0, IX1, and IX2) for 128-bit DTMOS ROM at transistor column 4 row 5

IV. CONCLUSION

In this paper, 128-bit standard ROM and 128-bit DTMOS ROM are simulated using ELDO for a comparison analysis. It is found from pre-silicon data that the power consumption for 128-bit DTMOS ROM is about 61.86% less compare to 128-bit standard ROM. The tradeoff comes in the form of die-area, as DTMOST circuit employs the deep n-well process, which utilizes 69% extra area. Both circuits are now being sent for fabrication at Silterra, and post-silicon measurement will be performed to validate this finding. This analysis shows low power consumptions can be achieved using DTMOS approach.

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